

Design and System Drivers

Technology Pacing Session

Worldwide Design ITWG

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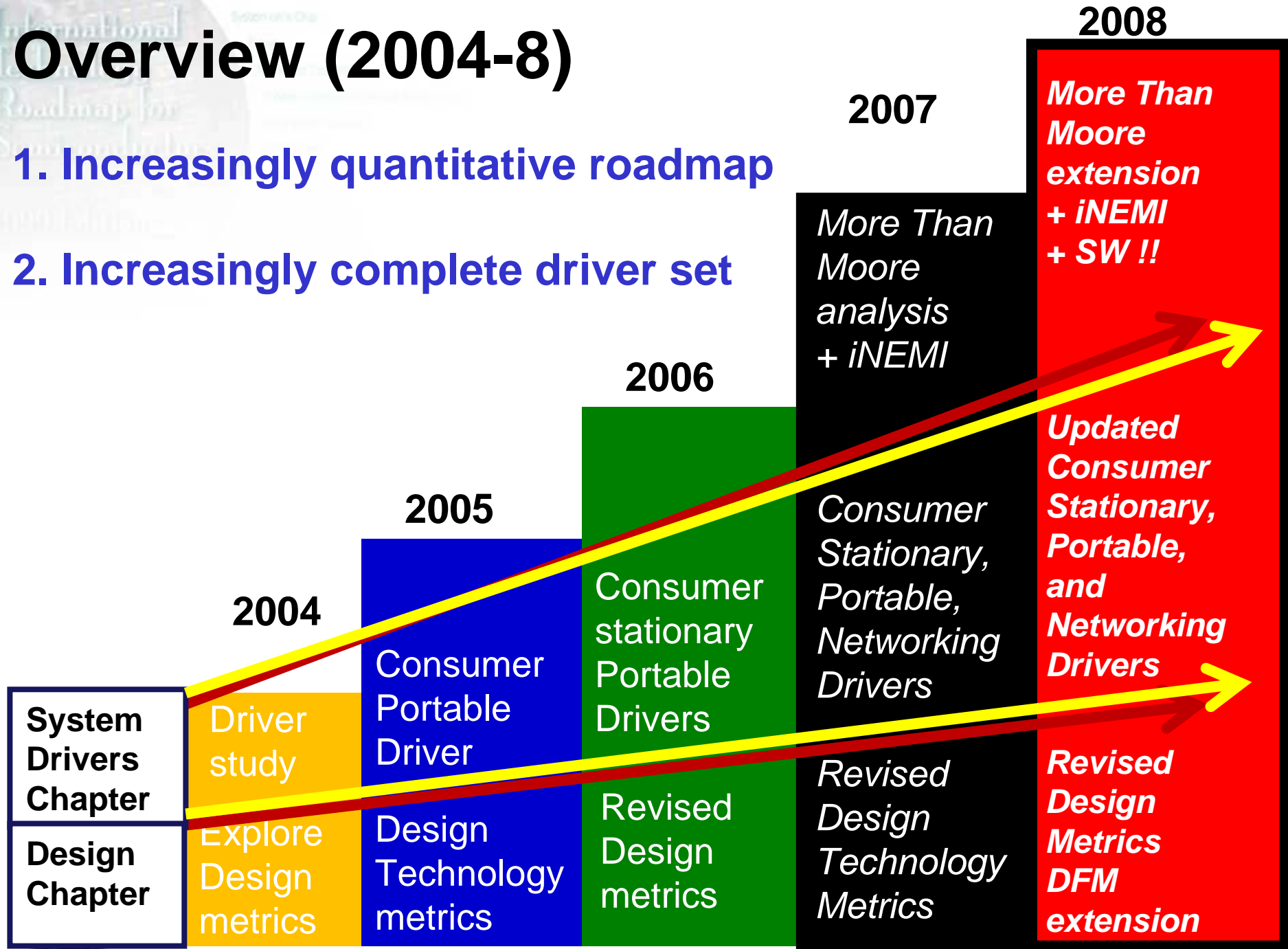
Key messages:

- 1.- Software is now an integral part of semiconductor products***
- 2.- Design increasingly enables viable technology control reqts***
- 3.- Design technology pacing largely unaffected by HP GL shift***
- 4.- Key system drivers updated in 2008 (MPU, Consumer P/S)***
- 5.- MtM brings a new set of Design requirements/solutions*
- 6.- MtM brings a new set of System Drivers' parameters*
- 7.- Will continue to broaden System Drivers based on markets*

Overview (2004-8)

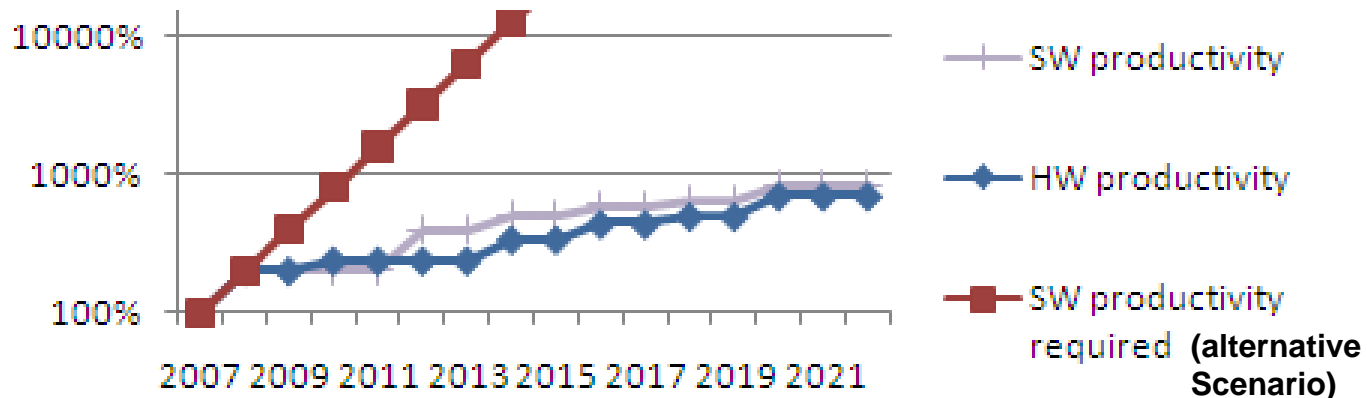
1. Increasingly quantitative roadmap

2. Increasingly complete driver set



System Level Design & SOFTWARE

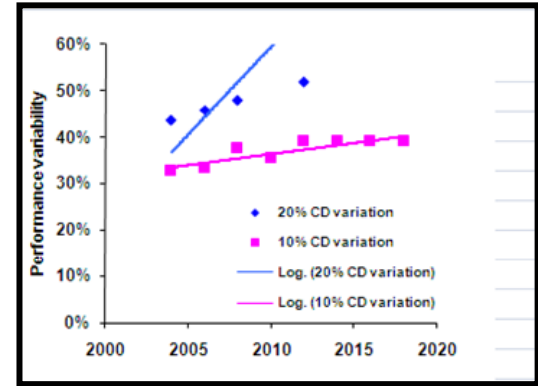
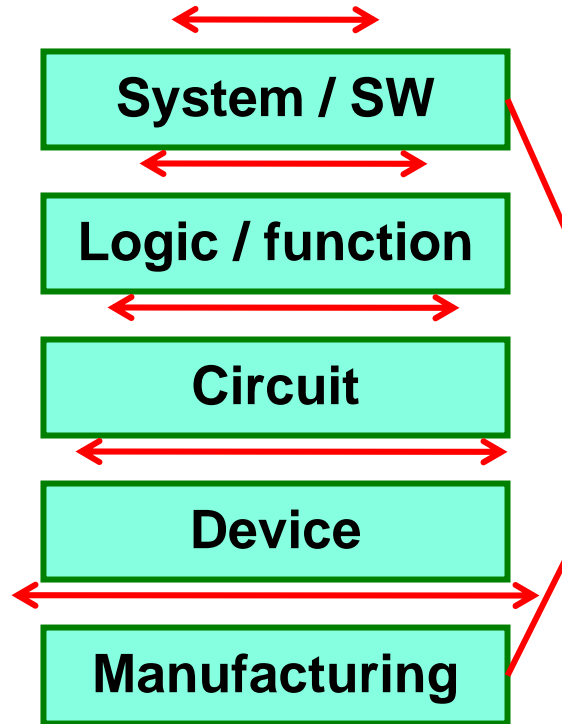
- **Hardware design productivity is growing appropriately**
 - Requirements correspond roughly with solutions
 - Innovations pacing properly (transistors / designer / year)
- **Large gap in software productivity possibly opening up**
 - If hardware accelerators are heavily leveraged, problem mitigated
 - Otherwise, possibly 100X gap can affect memory size, other
- **Adding new parameters to requirements/solutions tables**
 - Hardware design productivity - **requirement**
 - Software design productivity - **requirement**
 - Software design productivity (assuming only software implementation)
 - System design productivity innovations – **solutions** (Fig. 1 in chapter)



Impact of Design on "Sigma" (Variability)

- **Goal:**
 - Quantify "how many sigmas" can design "reduce"

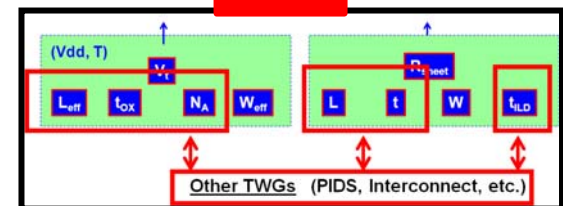
- **Approach**
 - Inventory of design techniques / tools
 - Match inventory to parameters or correlations in model
 - Use variability model to capture "delta" in sigmas



Check overall variation

	CD variation	CD % variation	delay variation	Power variation	Leakage power variation
2004	0.012	12%	44%	45%	123%
2006	0.0084	12%	46%	50%	201%
2008	0.00684	12%	48%	62%	240%
2010	0.00552	12%	61%	68%	289%
2012	0.0042	12%	52%	60%	306%
2014	0.00336	12%	77%	89%	397%
2016	0.00276	12%	89%	107%	335%
2018	0.00216	12%	93%	112%	551%
2020	0.00156	12%	115%	113%	545%
2022	0.00096	12%	126%	103%	548%

Use variability model



Inputs (manufacturing) 4

Technology Pacing (Design)

Impact of 3 year shift on Design

- Largely insignificant – number of functions basically unchanged
- Possible impact on selected requirements (e.g. DFM)

PIDS / FEP / Litho 3-year shift

Table FEP-4a
Grey cells indicate the requirements projected only for intermediate, or long-term years. Near-term line items are not included.

IS	Year of Production	2007	2008	2009	2010	2011	2012	2013	2014	2015
IS	MPU Physical Gate Length (nm)	32	28	21	24	22	20	18	17	15
IS	FORMULA	2003	04-03-06	04-06-07	04-07-08	04-09-09	2009	10-09	04-10-11	04-11-12
	Gate dielectric leakage at 100°C (A/cm ²) FDSOI high-performance [B, B1, B2]							1.10E+03	1200	1350
	Metal gate work function for FDSOI MPU/ASIC $\phi_m - B_1$ (eV) NMOS PMOS [S]							±0.15		
	Saturation velocity enhancement factor MPU/ASIC [T]	1	1				1.1	1.1		
	Si thickness FDSOI (nm) from PIDS [T]							5.5	5.35	4.85
	Maximum allowable parasitic series resistance for FDSOI NMOS MPU/ASIC * width (Ω-μm) [G]							180	160	180
	Maximum drain extension sheet resistance for FDSOI MPU/ASIC (NMOS) (Ω/sq) [G]							730	750	830
	Spacer thickness, FDSOI elevated contact [J]							8.9	8.25	8.25
	Thickness of FDSOI elevated junction (nm) [U]							18	17	15
	Maximum silicon consumption for FDSOI MPU/ASIC (nm) [K]							18	17	15
	Slide thickness for FDSOI MPU/ASIC (nm) [L]							22	20.5	18
	Contact silicide sheet R _c for FDSOI MPU/ASIC (Ω/sq) [M]							7.4	7.85	8.8
	Contact maximum resistivity for FDSOI MPU/ASIC (Ω-cm ⁻¹) [N]							7.20E-08	6.85E-08	6.15E-08
	Drench fill aspect ratio - FDSOI [V]							0.6	0.6	0.6
	Equivalent physical oxide thickness for multi-gate MPU/ASIC (nm) for metal gate (A, A1, A2)									0.75
	Gate dielectric leakage at 100°C (A/cm ²) multi-gate high-performance [B, B1, B2]									1340
	Metal gate work function for multi-gate MPU/ASIC [S]									
	Si thickness for multi-gate (nm) from PIDS [U]									9
	Maximum allowable parasitic series resistance for multi-gate NMOS MPU/ASIC * width (Ω-μm) [G]									180
	Maximum drain extension sheet resistance for multi-gate MPU/ASIC (NMOS) (Ω/sq) [G]									450
	Spacer thickness, multi-gate elevated contact [J]									8.25
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	Contact maximum resistivity for multi-gate MPU/ASIC (Ω-cm ⁻¹) [N]									6.35E-08

Updated Design requirements (DFM) (% variability model, etc.)

DFM requirements	comments	Near-term										Long-term									
		2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020				
Node		80	70	65	57	50	50	50	35	35	35	25	25	25	18	18	18				
Mask cost (\$m)	From publicly available data	1.5	2.2	3.0	4.5	6.0	9.0	12.0	18.0	24.0	36.0	48.0	72.0	96.0	144.0	192.0	288.0				
% Vdd variability	% variability seen at on-chip circuits	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%				
% Vth variability	Doping variability impacts VTH	24%	27%	31%	35%	40%	40%	58%	58%	58%	81%	81%	81%	81%	112%	112%	112%				
% Vth variability	Includes all sources	26%	29%	33%	37%	42%	42%	58%	58%	58%	81%	81%	81%	81%	112%	112%	112%				
% CD variability	CD for now, might add doping laser	10%	12%	12%	12%	12%	12%	12%	12%	12%	12%	12%	12%	12%	12%	12%	12%				
% circuit performance variability	circuit comprising gates and wires	41%	42%	45%	48%	49%	50%	52%	54%	57%	58%	61%	62%	65%	66%	69%	69%				
% circuit power variability	circuit comprising gates and wires	55%	55%	56%	56%	57%	57%	58%	58%	59%	59%	60%	60%	61%	61%	62%	62%				

Technology Pacing (System Drivers)

Impact of 3-year shift on System Drivers

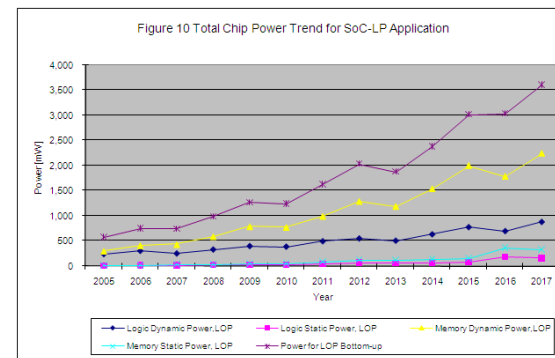
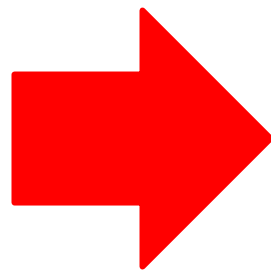
- MPU frequency model intact
- Consumer driver model: expect low or no impact
- Incorporate impact of FINAL parameters from 3-year shift - 2009

Updated Consumer portable (power)

PIDS / FEP / Litho 3-year shift

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IS	FOCUS/FLA	2003	06-03-06	08-06-07	08-07-08	08-09-09	2009	30-09	08-10-11	08-11-12
	Gate dielectric leakage at 100°C (A/cm ²) FDSOI high-performance [B, B1, B2]							1.10E+03	1200	1350
	Metal gate work function for FDSOI MPUASIC $\phi_m - B_1$ (eV) NMOS PMOS [S]							40.15		
	Saturation velocity enhancement factor MPUASIC [T]	1	1				1.1	1.1		
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Updated MPU model (power)

