

# **ITRS Public Conference**

## ***Emerging Research Devices***

### **San Francisco**

#### **Agenda**

- Technology Workshops**
- IRC Request**
- ERD/ERM Recommendation**

**Jim Hutchby – SRC**

**July 16, 2008**

# Emerging Research Devices Working Group

- ◆ Hiroyugi Akinaga
- ◆ Tetsuya Asai
- ◆ Yuji Awano
- ◆ George Bourianoff
- ◆ Michel Brillouet
- ◆ Joe Brewer
- ◆ John Carruthers
- ◆ Ralph Cavin
- ◆ U-In Chung
- ◆ An Chen
- ◆ Philippe Coronel
- ◆ Shamik Das
- ◆ Erik DeBenedictis
- ◆ Simon Deleonibus
- ◆ Kristin De Meyer
- ◆ Michael Frank
- ◆ Akira Fujiwara
- ◆ Christian Gamrat
- ◆ Mike Garner
- ◆ Dan Hammerstrom
- ◆ Wilfried Haensch
- ◆ Tsuyoshi Hasegawa
- ◆ Shigenori Hayashi
- ◆ Dan Herr
- ◆ Toshiro Hiramoto
- ◆ Matsuo Hidaka
- ◆ Jim Hutchby
- ◆ Adrian Ionescu
- ◆ Kohei Itoh
- ◆ Kiyoshi Kawabata
- ◆ Seiichiro Kawamura
- ◆ Rick Kiehl

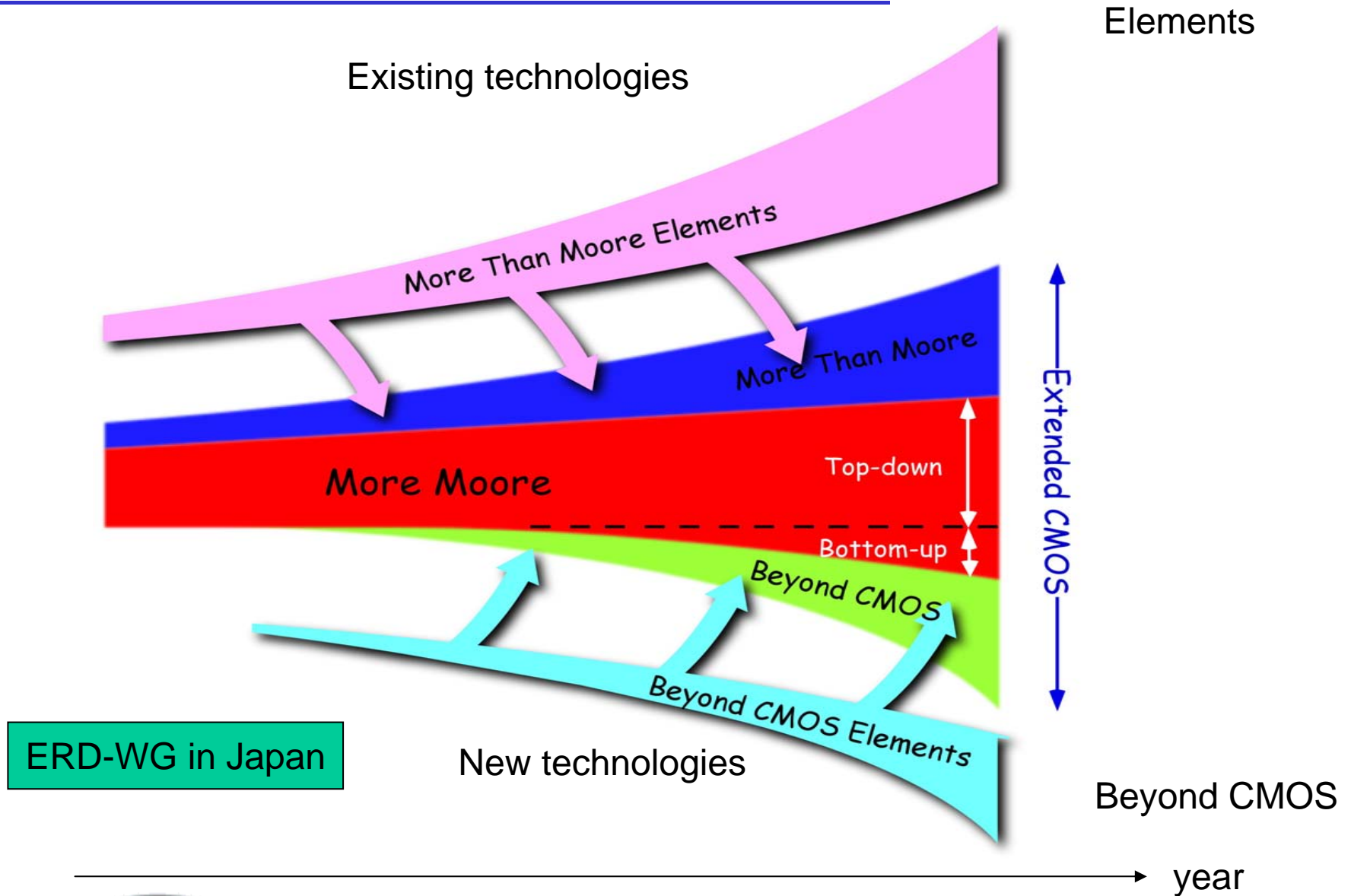
- AIST
- Hokkaido U.
- Fujitsu
- Intel
- CEA/LETI
- U. Florida
- PSU
- SRC
- Samsung
- AMD
- ST Me
- Mitre
- SNL
- LETI
- IMEC
- AMD
- NTT
- CEA
- Intel
- PSU
- IBM
- NIMS
- Matsushita
- SRC
- U. Tokyo
- ISTEK
- SRC
- ETH
- Keio U.
- Renesas Tech
- Selete
- U. Minn

- ◆ Hiroshi Kotaki
- ◆ Atsuhiko Kinoshita
- ◆ Franz Kreupl
- ◆ Nety Krishna
- ◆ Zoran Krivokapic
- ◆ Phil Kuekes
- ◆ Lou Lome
- ◆ Hiroshi Mizuta
- ◆ Murali Muralidhar
- ◆ Fumiyuki Nihei
- ◆ Dmitri Nikonov
- ◆ Wei-Xin Ni
- ◆ Ferdinand Peper
- ◆ Yaw Obeng
- ◆ Dave Roberts
- ◆ Kaushal Singh
- ◆ Sadas Shankar
- ◆ Thomas Skotnicki
- ◆ Satoshi Sugahara
- ◆ Shin-ichi Takagi
- ◆ Ken Uchida
- ◆ Yasuo Wada
- ◆ Rainer Waser
- ◆ Franz Widdershoven
- ◆ Jeff Welser
- ◆ Philip Wong
- ◆ Kojiro Yagami
- ◆ David Yeh
- ◆ In-Seok Yeo
- ◆ In-K Yoo
- ◆ Peter Zeitzoff
- ◆ Yuegang Zhang
- ◆ Victor Zhirnov

- Sharp
- Toshiba
- Qimonda
- AMAT
- AMD
- HP
- IDA
- U. Southampton
- Freescale
- NEC
- Intel
- NDL
- NICT
- NIST
- Air Products
- AMAT
- Intel
- ST Me
- Tokyo Tech
- U. Tokyo
- Toshiba
- Waseda U.
- RWTH A
- NXP
- NRI/IBM
- Stanford U.
- Sony
- SRC/TI
- Samsung
- SAIT
- Freescale
- Intel
- SRC



# Evolution of Extended CMOS



# 2008 ERD/ERM Workshops

Workshop topic	Date	Location	Meeting	Specific technology entries
Emerging Research Memory Devices	April 2 2008	Bonn, Germany	ITRS Spring meeting	<ul style="list-style-type: none"> <li>- Performance analysis for the various types of memories</li> <li>- Magnetic Race-Track Memory</li> <li>- Nanowire Phase-Change Memory</li> <li>- Polymer/Macromolecular Memory</li> </ul>
Emerging Research Architectures	July 10-11 2008	San Francisco, CA, USA	Semicon West	<ul style="list-style-type: none"> <li>- Chip Multiprocessors</li> <li>- Memory Architectures</li> <li>- Morpnic Computational Architectures</li> <li>- Turing-Heisenberg Rapprochement</li> </ul>
Evaluation of Beyond CMOS Logic Device Tech	July 12-13 2008	San Francisco, CA, USA	Semicon West	Evaluate Seven Logic Device Technologies to identify those ready for accelerated development
Emerging Research Logic Devices	Sept. 22 2008	Tokyo, Japan	SSDM	<ul style="list-style-type: none"> <li>- Nonlinear response functions</li> <li>- Devices for “functional diversification”?</li> <li>- Optimum circuit architectures associated with novel devices</li> </ul>
Emerging Research Materials	Nov. 10 2008	Austin, TX, USA	MMM*	Materials for Spintronic Devices <ul style="list-style-type: none"> <li>- Energetics</li> <li>- Transitions</li> <li>- Time scales</li> <li>- Interactions with external fields</li> </ul>
Emerging Research Materials	March 2009	Tokyo, Japan		Strongly Correlated Electron Materials

\* 53<sup>rd</sup> Magnetism and Magnetic Materials Conference

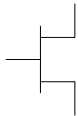
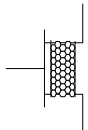
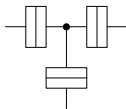
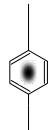

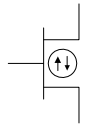
**Co-sponsored by the National Science Foundation**

# **International Roadmap Committee Request**

**Determine which, if any, current approaches to providing a “Beyond CMOS” information processing technology(ies) is (are) ready for more detailed roadmapping and enhanced investment.**

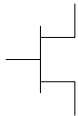
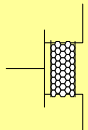
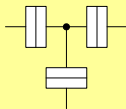
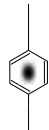

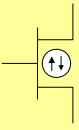
# 2007 ITRS ERD

## Emerging Research Logic Devices

<i>Device</i>							
		<i>FET Extension</i>					
	<i>FET [A]</i>	<i>ID structures</i>	<i>Channel replacement</i>	<i>SET</i>	<i>Molecular</i>	<i>Ferromagnetic logic</i>	<i>Spin transistor</i>
<i>Typical example devices</i>	Si CMOS	CNT FET NW FET NW hetero-structures Nanoribbon transistors with graphene	III-V compound semiconductor and Ge channel replacement	SET	Crossbar latch Molecular transistor Molecular QCA	Moving domain wall M: QCA	Spin Gain transistor Spin FET Spin Torque Transistor

# 2007 ITRS ERD

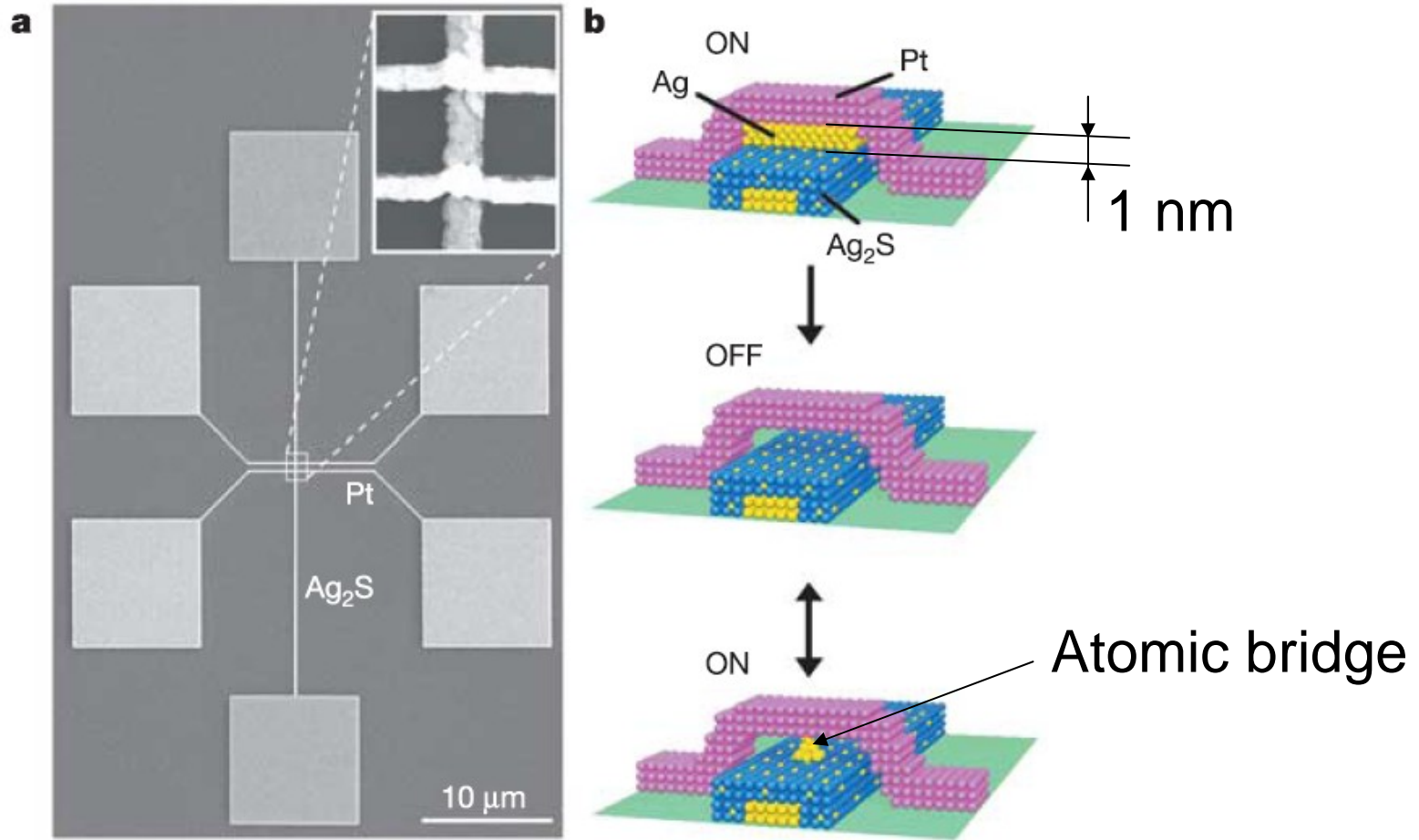
## Emerging Research Logic Devices Evaluated

<i>Device</i>							
		<i>FET Extension</i>					
	<i>FET [A]</i>	<i>ID structures</i>	<i>Channel replacement</i>	<i>SET</i>	<i>Molecular</i>	<i>Ferromagnetic logic</i>	<i>Spin transistor</i>
<i>Typical example devices</i>	Si CMOS	CNT FET NW FET NW hetero-structures Nanoribbon transistors with graphene	III-V compound semiconductor and Ge channel replacement	SET	Crossbar latch Molecular transistor Molecular QCA	Moving domain wall M: QCA	Spin Gain transistor Spin FET Spin Torque Transistor

# Emerging Research Device Technology Candidates Evaluated

- Nano-electro Mechanical Switches
- Collective Spin Devices
- Spin Torque Transfer Devices
- Atomic Switch / Electrochemical Metallization
- Carbon-based Nanoelectronics
- Single Electron Transistors
- CMOL / Field Programmable Nanowire Interconnect (FPNI)

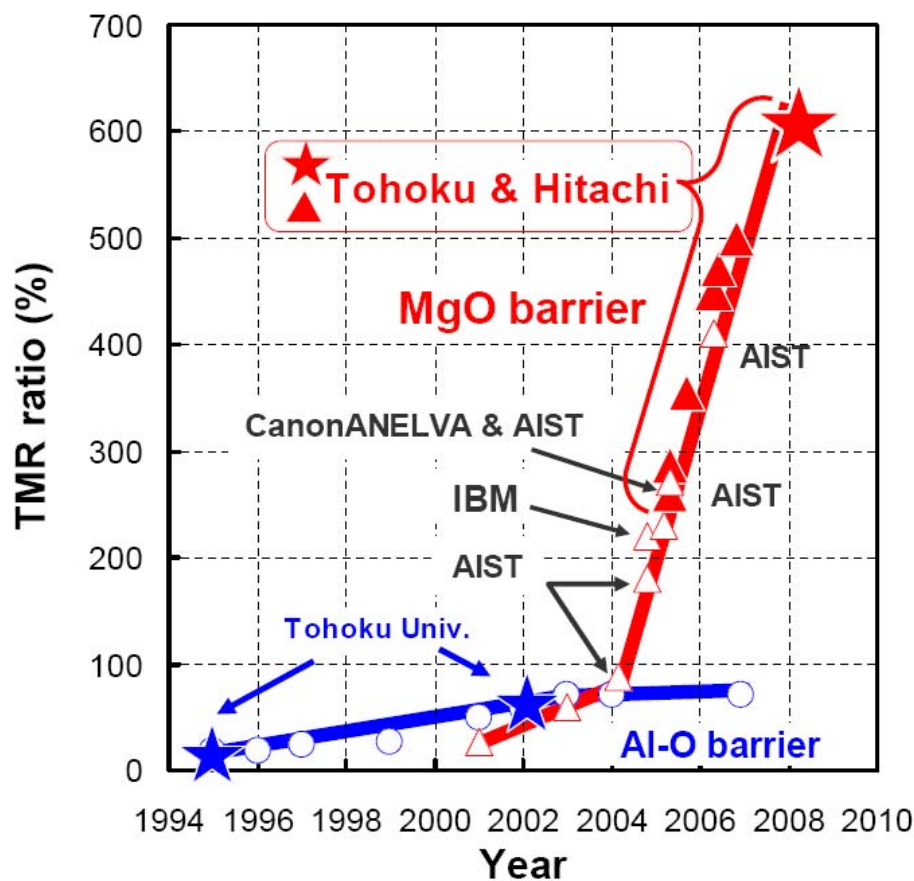
# Atomic Switch



K. Terabe et al. Nature 433 (2005) 47

# H. Ohno, “Spintronics”

Seminar, UCSB May, 2008

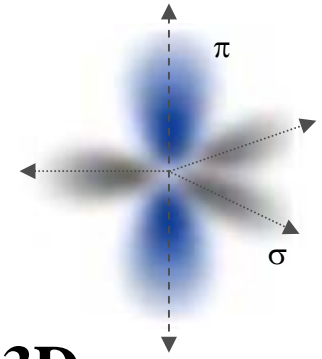


**604% @ 300K**  
**(1144% @ 5K)**

**Intermag 2008 HR-01**  
**S. Ikeda et al.**

For MgO barrier MTJs,  
AIST (S. Yuasa et al.): JJAP43(2004)L588, Nature Mater. 3(2005)868; APL89(2006)042505.  
IBM (S.S.P. Parkin et al.): Nature Mater. 3(2005)862.  
CanonANELVA & AIST: APL 86(2005) 092502  
Tohoku Univ. & Hitachi:  
JJAP44(2005)L587; JJAP44(2005)L1442;  
JAP99(2006)08A907; APL 89(2006)042506.  
APL89(2006)232510; APL90(2007)212507.  
IEEE T-ED 54(2007)991.

# SP<sub>2</sub> Carbon: 0-Dimension to 3-Dimension



Atomic orbital sp<sub>2</sub>

0D

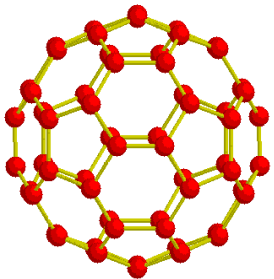
1D

2D

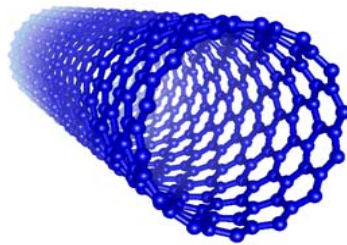
3D



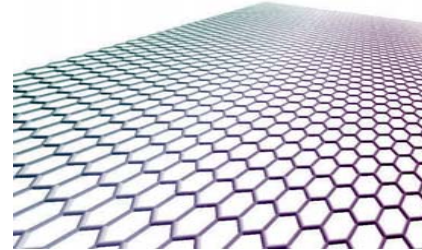
Fullerenes (C<sub>60</sub>)



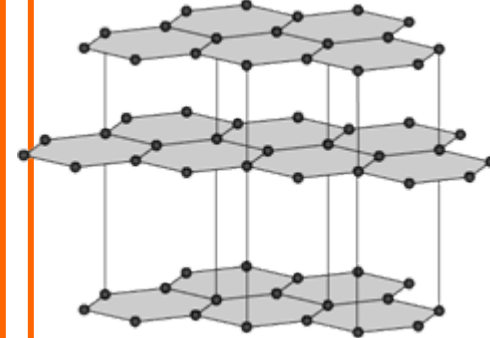
Carbon Nanotubes



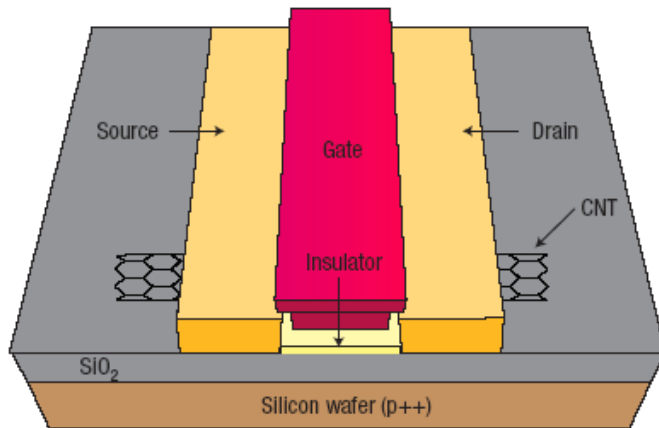
Graphene



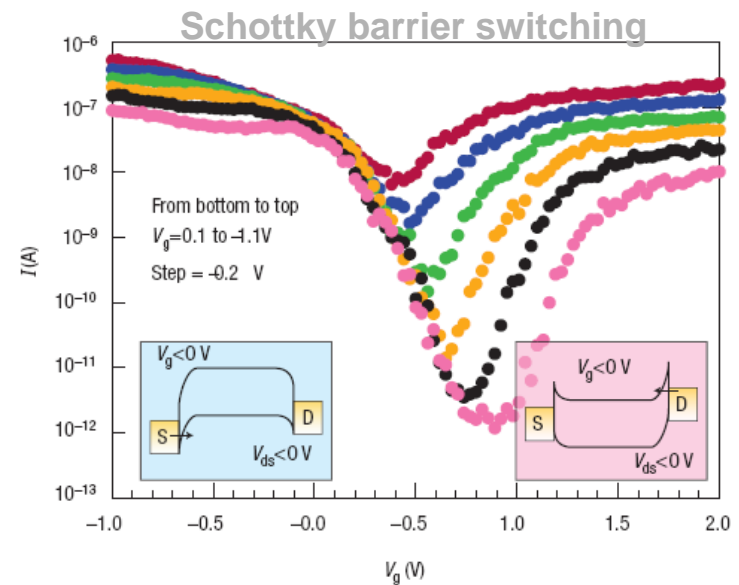
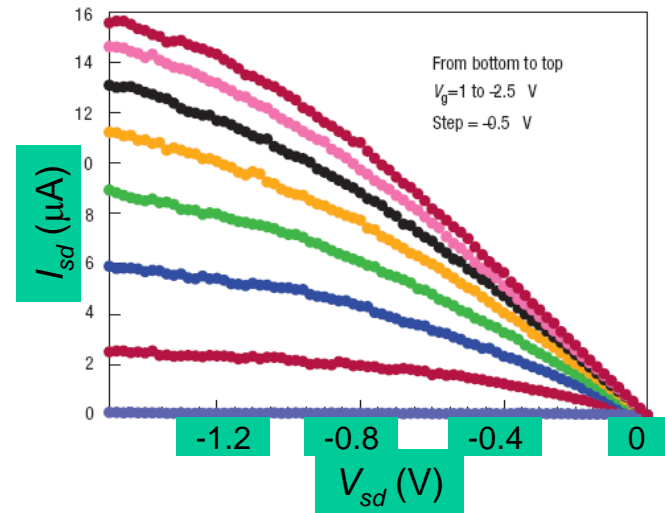
Graphite



# Nanotube FET



Band gap: 0.5 – 1 eV  
 On-off ratio:  $\sim 10^6$   
 Mobility:  $\sim 100,000 \text{ cm}^2/\text{Vsec}$  @RT  
 Ballistic @RT  $\sim 300\text{-}500 \text{ nm}$   
 Fermi velocity:  $10^6 \text{ m/sec}$   
 Max current density  $> 10^9 \text{ A/cm}^2$



Ph. Avouris et al, Nature Nanotechnology 2, 605 (2007)

# ERD/ERM TWG Recommendation

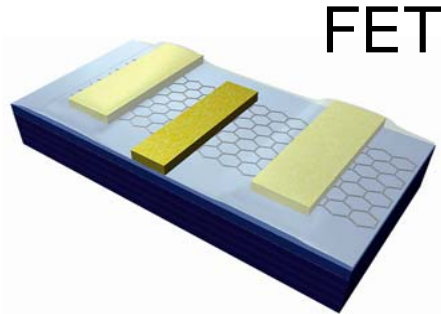
**The ERD/ERM TWGs recommend to the  
International Roadmap Committee ---**

**Carbon-based Nanoelectronics to  
include carbon nanotubes and  
graphene**

**For additional resources and detailed road  
mapping for ITRS as promising technologies  
targeting commercial demonstration in the 5-10  
year horizon.**

# Graphene Electronics: Conventional & Non-conventional

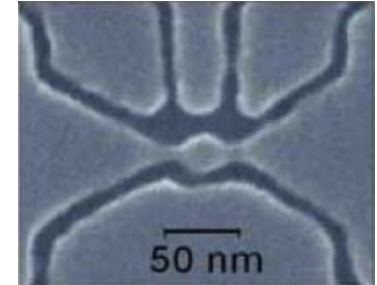
## Conventional Devices



FET

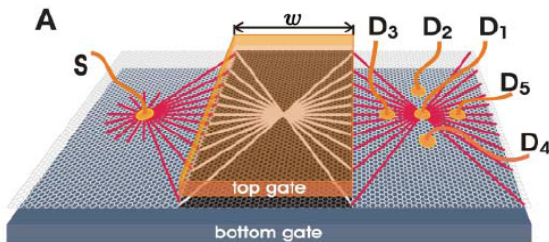
Leverage R & D

Graphene quantum dot



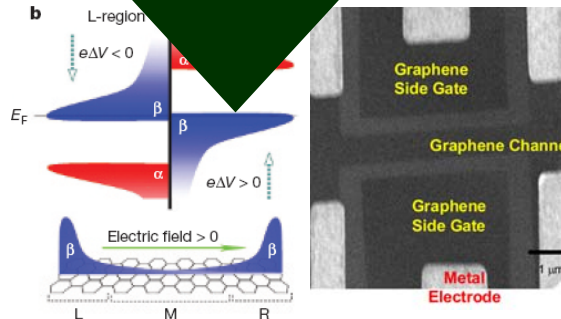
(Manchester group)

## Nonconventional Devices



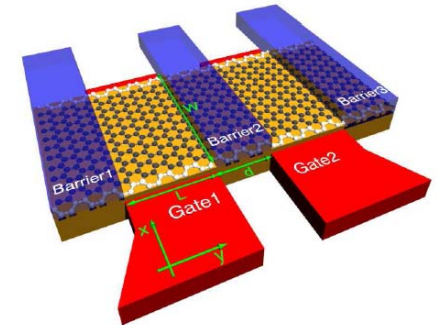
Graphene Veselago lense

Cheianov *et al. Science* (07)



Graphene Spintronics

Son *et al. Nature* (07)



Graphene pseudospintronics

Trauzettel *et al. Nature Phys.* (07)

# Advantages

## Carbon-based Nanoelectronics ---

**For scaled CMOS, potentially can ..**

- ◆ **Impact geometric scaling by providing an alternate MOSFET structure, and**
- ◆ **Provide a high mobility, high carrier velocity, MOSFET channel replacement material.**

**For a new information process technology, potentially can ...**

- ◆ **Leverage R & D for CMOS (above) to ...**
- ◆ **Provide a technology platform enabling a new “Beyond CMOS” information processing paradigm**



# **Caveat Carbon-based Nanoelectronics**

**The intent of this recommendation is to highlight Carbon-based Nanoelectronics for additional roadmapping and investment ---**

**--- but not at the expense of investment in or exploration of other candidate approaches for “Beyond CMOS” information processing technology.**

**We are not picking winners and losers**

# Summary

- Preparing for 2009 ERD Chapter re-write
- Conducting six workshops in collaboration with NSF, SRC, and ERM (Three accomplished)
  - Evaluate technology entries for 2009
  - Respond to IRC request (see next bullet)
- Responded to IRC request to identify one or more Beyond CMOS technologies for road mapping and enhanced investment
  - Conducted in-depth evaluation of seven Beyond CMOS technologies (including one device architecture)
  - Recommended Carbon-based Nanoelectronics to IRC

# **Backup Slides**

## **Objectives and Agendas of the ERD/ERM Technology Workshops**

# 2008 ERD/ERM Workshops

Workshop topic	Date	Location	Meeting	Specific technology entries
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\* 53<sup>rd</sup> Magnetism and Magnetic Materials Conference

**Co-sponsored by the National Science Foundation**

# ERD ITWG

*Emerging Research Devices*

*Working Group*

**Face-to-Face Meeting**

**MEMORY DISCUSSION**

Victor Zhirnov and Rainer Waser - Facilitating  
Grand Hotel Steigenburger Petersberg

**Rheinblick**

Koenigswinter (near Bonn), Germany

Wednesday April 2, 2008

8:00 a.m. – 1:30 p.m

# Objectives

- **To develop quantitative estimates of performance for the various types of memories**
  - We need to discuss and agree on the methodology we use and the numbers we obtained
  - It is highly desirable to document the results, ideally as a journal publication
- **To discuss new possible memory candidates**

# ERD ITWG Memory Discussion Agenda

- |       |  |                      |
|-------|--|----------------------|
| 8:00  | Review meeting objectives and agenda   | Hutchby              |
| 8:15  | Introductory remarks on Memory Discussion                                      | Zhirnov              |
| 8:30  | Nanowire Phase-change memory   | Meyyapan             |
| 9:30  | Magnetic Race-Track & Spin-torque Transfer Memories                            | Zhirnov              |
| 10:30 | Break  |                      |
| 10:45 | <b>Quantitative estimates of performance for the various types of memories</b> |                      |
|       | <input type="checkbox"/> Engineered barrier                                    | Muralidhar & Zhirnov |
|       | <input type="checkbox"/> Ferroelectric   | Waser                |
|       | <input type="checkbox"/> Nanoelectromechanical                                 | Zhirnov              |
|       | <input type="checkbox"/> Fuse/Antifuse   | Waser & Akinaga      |
| 12:00 | Lunch  |                      |
| 12:30 | <b>Continue quantitative estimates .....</b>                                   |                      |
|       | <input type="checkbox"/> Ionic   | Waser & Akinaga      |
|       | <input type="checkbox"/> Electronic Effects                                    | Waser                |
|       | <input type="checkbox"/> Macromolecular  | Zhirnov              |
|       | <input type="checkbox"/> Molecular   | Waser                |
| 1:30  | <b>Break - Adjourn Memory Discussion</b>                                       |                      |
| 2:00  | <b>ERD Business Meeting</b>  |                      |



# **SRC/NSF/ITRS Forum on Emerging nano-CMOS Architectures in Conjunction with Frontiers of Extreme Computing 2008: 2020 Virtual Immersion Architectures**

**July 10-11, 2008**

**Univ. of California/Santa Cruz, Seymour Marine Discovery Center at Long Marine Laboratory, La Feliz Room**

**Santa Cruz, California**

This forum is to explore the potential capabilities and applications of virtual immersion technologies given extremely scaled CMOS devices. Please note that the deadline for registering for this event is **Friday, June 27, 2008**

## **Expected Outcome**

Definition of promising research directions to enable virtual immersion applications in the 2020 timeframe.

# ITRS/ERD ITWG

## Emerging Research Devices Work Group

### *Workshop & Work Group Meeting*

### *Evaluation of Selected Beyond CMOS Emerging Technologies*

Jim Hutchby - Facilitating

San Francisco Marriott Hotel

55 Fourth Street, San Francisco, CA

**Nob Hill D Room**

**Yerba Buena Level**

Saturday, July 12 (Workshop)

8:00 a.m. – 10:00 p.m.

Sunday, July 13 (ERD Working Group Meeting)

9:00 a.m. – 5:45 p.m.

# Objectives

## **Workshop (For each of the seven technologies)**

- Receive expert inputs on the seven technologies for future information processing (pro & con)
- Clarify status, potential, and remaining challenges
- Formulate discussion/decision points to be considered in the Sunday ERD/TWG meeting
- Consider if one or more of the seven candidate technologies is ready for enhanced engineering development and detailed roadmapping (Sunday)

# Information Requested (1/2)

- ◆ **Proposed device technology (device, physics, interconnect, input/output functions)**
  - “Beyond CMOS” technologies that extend the functional scaling of CMOS beyond that attainable with dimensional scaling
  - Device technologies that provide a new “Beyond CMOS” paradigm for highly scalable information processing
- ◆ **Scaling potential (device or functional density) compared to ultimately scaled CMOS)**
  - Geometric (size, density, etc.)
  - Dissipated power density (dynamic, static, ...)

# Information Requested (2/2)

- ◆ **Projected performance (power, speed, gain, throughput per Joule, etc. ...) at maturity**
- ◆ **Reduction to practice - status**
  - Demonstration of “proof-of-concept” of device, unit cell and functional circuit
  - Fabrication technology – challenges
  - Progress in past four years
- ◆ **Current state-of-the-art using the provided metrics as a guide (Appendix 2 of request for white papers)**
- ◆ **Key scientific and technological issues remaining to accept the technology for manufacture.**
- ◆ **Technology roadmap outlining a 5-15 year develop path leading to manufacture in 5-10 years.**

# **“Beyond CMOS” Technology Maturity Workshop**

## **Agenda – Saturday, July 12**

- 8:00 Welcome and Introductions** Hutchby
- 8:10 Background, Workshop & ERD Meeting Objectives** Hutchby
- 8:20 NEMS Switch Technology**
- Proponent Presentation (40 minutes) Akarvardar
  - Friendly Critic Presentation (20 minutes) Elata
  - Discussion for clarification (20 minutes)
- 9:40 Spin Torque Transfer Technology**
- Proponent Presentation (40 minutes) Allen
  - Friendly Critic Presentation (20 minutes) Yablonovitch
  - Discussion for Clarification (20 minutes)
- 11:00 Break**
- 11:20 Carbon-based Nanoelectronics**
- Proponent Presentation (40 minutes) Kim
  - Friendly Critic Presentation (20 minutes) Javey
  - Discussion for Clarification (20 minutes)
- 12:40 Lunch (Working)**

# “Beyond CMOS” Technology Maturity Workshop

## Agenda – Saturday, July 12 (Cont’d)

### 1:10 Atomic Switch / Electrochemical Metal Switch

- Proponent Presentation (40 minutes) Kuekes
- Friendly Critic Presentation (20 minutes) Chen
- Discussion for Clarification (20 minutes)

### 2:30 Collective Spin Devices (including M-QCA)

- Proponent Presentation (40 minutes) Wang
- Friendly Critic Presentation (20 minutes) Bandyopadhyay
- Discussion for Clarification (20 minutes)

### 3:50 Break

### 4:10 Single Electron Transistors

- Proponent Presentation (40 minutes) Fujiwara
- Friendly Critic Presentation (20 minutes) Likharev
- Discussion for Clarification (20 minutes)

### 5:30 CMOL and FPNI

- Proponent Presentation (40 minutes) Likharev
- Friendly Critic Presentation (20 minutes) DeHon
- Discussion for Clarification (20 minutes)

### 6:50 Dinner Break (Return @ 8:00 p.m.)

# **“Beyond CMOS” Technology Maturity Workshop**

## **Agenda – Saturday, July 12 (Cont’d)**

- |              |   |                     |
|--------------|---|---------------------|
| <b>8:00</b>  | <b>Summary Session – introduction &amp; Objective</b> | <b>Hutchby</b>      |
| <b>8:10</b>  | <b>NEMS Switch</b>                                    | <b>Franzon</b>      |
| <b>8:25</b>  | <b>Spin Transfer Torque</b>                           | <b>Bourianoff</b>   |
| <b>8:40</b>  | <b>Carbon-based Nanoelectronics</b>                   | <b>Brillouet</b>    |
| <b>8:55</b>  | <b>Atomic Switch / Electrochemical Metal Switch</b>   | <b>Haensch</b>      |
| <b>9:10</b>  | <b>Collective Spin Devices (including M-QCA)</b>      | <b>Shankar</b>      |
| <b>9:25</b>  | <b>Single Electron Transistors</b>                    | <b>Hiramoto</b>     |
| <b>9:40</b>  | <b>CMOL and FPNI</b>                                  | <b>DeBenedictis</b> |
| <b>10:00</b> | <b>Adjourn</b>  |                     |

**\* Volunteer Discussion Leaders Needed**