2009 iedm

international Electron Devices meeting

Hilton Baltimore
Baltimore, MD
December 7-9, 2009

Sponsored by
Electron Devices Society of IEEE

WELCOME FROM THE GENERAL CHAIR

On behalf of the entire IEDM committee, I would like to welcome you to the 2009 IEEE International Electron Devices Meeting to be held December 7-9, 2009 in Baltimore, MD. The IEDM continues to be the world's premier venue for presenting the latest breakthroughs and the broadest and best technical information in electronic device technologies. This year we have a strong collection of both contributed and invited papers that will be presented by industrial and academic leaders and students from around the world. Short summaries of each paper are available on the IEDM web site, which we encourage everyone to visit – http://www.ieee.org/conference/iedm. This year, we will be distributing an abbreviated digest at the meeting, along with electronic versions of the complete abstracts, to more effectively leverage modern electronic content distribution capabilities. The full digest will be available on the IEEE Xplore website and the DVD package offered by the IEEE Electron Devices Society after the conference.

Vivek Subramanian
General Chair

In addition to the many regular paper sessions - and the always informative and entertaining IEDM Luncheon on Tuesday - we will again feature several special sessions.

On Sunday December 6, 2009, two short courses will be offered: "Low Power / Low Energy Circuits: From Device to System Aspects" and "Scaling Challenges: Device Architectures, New Materials, and Process Technologies". These courses have been organized and will be presented by internationally-known leading researchers active in their respective areas of technology. The topics have broad appeal to IEDM participants with material suitable for newcomers as well as experts in the field.

The Plenary Session on Monday morning will feature three invited talks: John Chen from nVidia will give a talk entitled "GPU Technology Trends and Future Requirements", Prof. Takao Someya from the University of Tokyo will present a talk entitled "Printed Organic Transistors: Toward Ambient Electronics". The final talk of the session will be provided by Jean Chabbal from CEA LETI, who will give a talk entitled "New Perspectives from Micro and Nanotechnologies in Healthcare and Diagnosis".

Meikei Ieong
Technical Program
Chair

The Luncheon on Tuesday will be given by Dr. Pushkar Apte, the Vice President of Technology Programs at the Semiconductor Industry Association. His stimulating talk is entitled "Semiconductor Industry: Inflection and Innovation".

On Tuesday night, we will again feature our popular and interactive Panel sessions. The first panel is entitled "Managing Innovation: An Oxymoron?", and will be organized by Jeff Welser from IBM and Rakesh Kumar from TCX Inc. This special panel is organized in cooperation with the IEEE Technology Management Council. The second panel is entitled "When and How Will the High Mobility Substrates Impact the Si Technology Roadmap?" This panel will be organized by Prof. Dimitri Antoniadis from MIT.

Recognizing the success of last year's special track on "device/circuit interaction", we will continue to offer this track this year, culminating in a special section on Tuesday afternoon, entitled "Confluence of Technology and Design: Design Issues at 32/22nm and Beyond".

The Emerging Technology special session this year features breakthroughs in "Graphene Nanoelectronics", and will include six talks from leading experts in this exciting new area looking from a broad variety of perspectives including materials, technology development, and modeling.
On behalf of the IEDM, Meikei Ieong, the Technical Program Chair, Kazunari Ishimaru, the Technical Program Vice-Chair, and I want to express our sincere appreciation to all of the IEDM authors and to each of the members of the IEDM committee. The authors really make the IEDM what it is; a forum for the presentation of the leading work in our field. The IEDM committee members did an outstanding job in planning and organizing the 2009 conference.

Kazunari Ishimaru
Technical Program
Vice Chair

The IEDM is sponsored by the IEEE Electron Devices Society. If you are not already an IEEE member, please consider joining this great institution which has played such an important role globally for over 120 years. More detailed information regarding the IEEE is available at this conference and on their website – http://www.ieee.org

It is again my great honor and pleasure to extend a warm welcome to everyone attending the 2009 IEEE International Electron Devices Meeting.

Vivek Subramanian
General Chair

Conference Highlights

SHORT COURSES
Sunday, December 6, 9:00 am – 5:30 p.m.
Key Ballroom 3, 4, 6
Key Ballroom 8, 11, 12

PLENARY SESSION
Monday, December 7, 9:00 am – 12:00 p.m.
Key Ballrooms 7 – 12

Plenary Session Award Presentations

2008 Roger A. Haken Best Student Paper Award

To: Jianqiang Lin, National University of Singapore

For the paper entitled, "Plasma PH3-Passivated High Mobility Inversion InGaAs MOSFET Fabricated with Self-Aligned Gate First Process and HfO_2/TaN Gate Stack."

2009 EDS Chapter of the Year Award

To: To Be Announced

"To an EDS chapter based on the quantity and quality of the activities and programs implemented by the chapter."

2009 EDS PhD Student Fellowship

To: Faisal Amir, The University of Manchester, Pierre-Yves Delaunay, Northwestern University, Ximeng (Simon) Guan, Tsinghua University, Rinus Tek Po Lee, National University of Singapore

"To promote, recognize, and support PhD level study and research within the Electron Devices Society's field of interest"

2008 EDS George E. Smith Award

To: H.S. Tan, T. Cahyadi, Z.B. Wang, A. Lohani, S.G. Mhaisalkar, Z. Tsakadze, S. Zhang, R.R. Zhu, D-H Kim, J-H Ahn, H-S Kim, K.J. Lee, T-H Kim, J.A. Rogers, C.J. Yu, R.G. Nuzzo

For the papers entitled: "Low-Temperature-Processed Inorganic Gate Dielectrics for Plastic-Substrate-Based Organic Field-Effect Transistors", and "Complementary Logic Gates and Ring Oscillators on Plastic Substrates by Use of Printed Ribbons of Single-Crystalline Silicon"

2008 EDS Paul Rappaport Award

To: K-W Ang, J. Q. Lin, G. S. Samudra, S-H Tung, N. Balasubramian, Y-C Yeo

For the paper entitled: "Strained n-MOSFET with Embedded Source/Drain Stressors and Strain-Transfer Structure (STS) for Enhanced Transistor Performance"

2009 IEEE/EDS Fellows

(Only includes those who requested to be recognized at the IEDM)

Rashid Bashir, University of Illinois at Urbana-Champaign, Champaign, IL
Tahir Ghani, Intel Corporation, Hillsboro, OR
Andrea Lacaita, Politecnico di Milano, Milano, Italy
Ching-Ting Lee, National Cheng Kung University, Tainan, Taiwan
Joe McPherson, Silicon Technology Development, Dallas, TX
Mehmet Ozturk, North Carolina State University, Raleigh, NC
Matthias Passlack, Freescale Semiconductor, Inc., Chandler, AZ
Mark Reed, Yale University, New Haven, CT
Adam Skorek, University of Quebec at Trois-Rivieres, Canada
Richard Swanson, SunPower Corporation, San Jose, CA
William Tonti, IEEE, Piscataway, NJ
Robert Wallace, University of Texas at Dallas, Richardson, TX
Albert Wang, University of California, Riverside, Riverside, CA
John Zolper, Raytheon, Vienna, VA

2009 EDS Distinguished Service Award:

To: Tak Ning, IBM T.J. Watson Research Center

"To recognize and honor outstanding service to the Electron Devices Society."

2009 EDS Education Award:

To: David Pulfrey, University of British Columbia

"For contributions to the teaching of semiconductor devices at both the undergraduate and graduate levels"

2009 EDS J.J. Ebers Award

To: Baruch Levush, National Research Lab

"For contributions to the development of widely applied simulation tools in the vacuum electronics industry"

RECEPTION

Monday, December 7, 6:00 p.m. – 8:00 p.m.
Holiday Ballroom 1-6

IEDM LUNCHEON

Tuesday, December 8
12:20 p.m. – 2:00 p.m.
Holiday Ballroom 4-6

2009 IEEE Cledo Brunetti Award

To: Bum J. Lin, TSMC
"For contributions to immersion lithography for the manufacture of integrated circuit devices"

2009 IEEE Andrew S. Grove Award

To: Eric Fossum.
"For significant contributions to the invention, development and commercialization of CMOS image sensors"

2009 IEEE Reynold B. Johnson Data Storage Device Technology Award

To: Kinam Kim, Samsung Electronics
"For leadership in and contribution to semiconductor memory technology which enabled the growth of low cost consumer data storage devices"

2009 IEEE Frederik Philips Award

To: Shojiro Asai, Rigaku Corporation
"For leadership in research and development in electron device technologies and their applications"

2009 IEEE Undergraduate Teaching Award

To: John C. Bean, University of Virginia
"For providing opportunities to both undergraduate and pre-college students for discovery through both laboratory projects and virtual experiments on the world wide web."

LUNCHEON PRESENTATION

"Semiconductor Industry: Inflection and Innovation"
Pushkar Apte, Semiconductor Industry Association

EVENING PANEL SESSIONS

Tuesday, December 8
8:00 p.m. - 10:00 p.m.
Key Ballroom 7, 9, 10
Key Ballroom 8, 11, 12

GENERAL INFORMATION

Hilton Baltimore
401 West Pratt Street
Baltimore, MD 21201
December 7 - 9, 2009

REGISTRATION INFORMATION

	Advance (Postmarked by November 16th)	After (November 16th or at Conference)
Technical Session		
IEEE Member	$425.00	$465.00
Non-member	$565.00	$605.00
Students:		
Member	$ 75.00	$ 75.00
Non-Member	$ 125.00	$ 125.00

Short Courses (Due to limited space, it is recommended that you register in advance for the Short Courses)

Member	$425.00
Non-member	$500.00
Student Member	$100.00
Student Non-Member	$150.00

If you are not already an IEEE and EDS member, we encourage you to join. You can either apply online at www.ieee.org/join/ or request an application form by sending an email to eds@ieee.org.

Payment of the Technical Session registration fee entitles the registrant to one copy of the Technical Digest on a USB drive, one ticket for the Monday evening Wine and Cheese Reception and entrance to all technical sessions. Technical Session registration does not include entrance to the Short Courses or the Tuesday Luncheon. TO QUALIFY FOR THE MEMBER REGISTRATION FEE, REGISTRANT MUST BE A MEMBER OF IEEE PRIOR TO THE CONFERENCE.

Payment of the Short Course registration fee entitles the registrant to entrance to one short course, and one copy of the course workbook, and short course cd-rom. Short Course registration does not include entrance to the Technical Sessions.

For Advance Registration, go to www.ieee.org/conference/iedm and click on "Register". Due to limited space, it is recommended that you register in advance to attend the Short Courses.

Confirmations will be sent out to all conference registrants.

REGISTRATION FORM AND PAYMENT SHOULD BE SENT TO:

IEDM
19803 Laurel Valley Place
Montgomery Village, MD 20886 USA
Tel: 301-527-0900 ext. 2
Fax: 301-527-0994

Checks **MUST BE MADE PAYABLE TO IEDM, IN U.S. DOLLARS AND DRAWN ON A U.S. BANK.** International registrants should not send wire transfers. If international participants cannot send a check prior to the conference, mail the registration form without payment prior to the conference. Bring payment with you and pay the registration fee onsite.

Your registration materials will be held for you at the conference. Your cancelled check is your receipt.

CANCELLATION POLICY: You are encouraged to register in advance for your own convenience. Due to printing and hotel commitments, refunds requested after November 16 cannot be guaranteed. A $30.00 processing fee will be withheld from ALL refunds.

REGISTRATION CENTER: The Conference Registration Center, located in the South Foyer of the Hilton Baltimore will be open as follows:

SHORT COURSE REGISTRANTS ONLY

Saturday, December 5	5:00 p.m. - 7:00 p.m.
Sunday, December 6	8:00 a.m. - 11:00 a.m.

TECHNICAL SESSION REGISTRANTS

Sunday, December 6	11:00 a.m. - 5:00 p.m.
Monday, December 7	8:00 a.m. - 5:00 p.m.
Tuesday, December 8	8:30 a.m. - 5:00 p.m.
Wednesday, December 9	8:30 a.m. - 3:00 p.m.

HOTEL RESERVATIONS: A block of rooms at the Hilton Baltimore has been reserved for IEDM participants. Special IEDM room rates are as follows:

Single/Double: $199

Plus a 13.05% city tax.

Please make your hotel reservation NO LATER THAN NOVEMBER 6th to qualify for a room under our special rates. An advance deposit or credit card guarantee is necessary to hold your room, if arrival is scheduled after 6:00 p.m.

SHORT COURSES: The IEDM sponsors two short courses on Sunday, December 6, from 9 a.m. to 5:30 p.m. The courses are "Low Power / Low Energy Circuits: From Device to System Aspects" and "Scaling Challenges: Device Architectures, New Materials, and Process Technologies". These courses will be presented by experts in the fields. Lectures will start with introductory material for the general audience and progress towards description of the latest developments.

To register, complete the Advance Registration form. The registration fee is $425 for members and $500 for non-members. It includes a visuals booklet, cd-rom, refreshments and lunch. Attendance is limited, so advance registration is recommended.

EVENING PANEL DISCUSSION: On Tuesday evening, December 8, beginning at 8:00 p.m. the IEDM will offer two evening Panel Discussions on "Managing Innovation: An Oxymoron?" and "When and How Will the High Mobility Substrates Impact the Si Technology Roadmap"

TO PERMIT SPONTANEOUS AND CANDID DISCUSSION, NO VERBATIM RECORDING BY TAPE OR CAMERA WILL BE PERMITTED DURING THE SHORT COURSES, TECHNICAL SESSIONS OR PANEL DISCUSSIONS.

SPEAKER PREPARATION ROOM: The IEDM will sponsor a Speaker Preparation Room in the Blake Room for speakers to preview their presentations. Speakers must preview their presentations one day in advance. There will be no previewing of presentations the day of the presentation.

The Speaker Preparation Room will be open for speaker use:

Saturday, December 5	5:00 p.m. - 7:00 p.m.
Sunday, December 6	8:00 a.m. - 5:00 p.m.
Monday, December 7	8:00 a.m. - 5:00 p.m.
Tuesday, December 8	8:00 a.m. - 5:00 p.m.
Wednesday, December 9	8:00 a.m. - 12:00 p.m.

IEDM LUNCHEON: The IEDM luncheon, featuring a presentation by Pushkar Apte, of the Semiconductor Industry Association on "Semiconductor Industry: Inflection and Innovation" will be held on Tuesday, December 8 at 12:20 p.m. in the Holiday Ballroom 4-6. Luncheon tickets are available through Advance Registration or on-site at a cost of $55.00.

WINE AND CHEESE RECEPTION: A Wine and Cheese Reception for conference participants and their guests will be held on Monday, December 7 from 6:00 p.m. to 7:30 p.m. ONE ADMISSION TO THE RECEPTION IS INCLUDED IN THE REGISTRATION FEE.

TECHNICAL DIGEST/CD-ROM: This year IEDM will not be producing a printed version of the digest. The digest will only be on a USB drive. If you are interested in a printed version of the digest, you may order and pay for it in advance on the registration form and it will be printed and mailed after the conference. Availability of the printed digest after the conference is subject to the number of pre-orders we receive. If the preorder is significantly low, prohibiting a cost effective print run, IEDM will refund the money to anyone who ordered a printed version of the digest.

GRADUATES OF THE LAST DECADE (GOLD): ***Your career and Networking with IEEE Electron Devices Society Adcom Members*** come join us on Sunday evening, December 6, 2009, 5:00-7:00 p.m. at the Hilton Baltimore Hotel for a free EDS sponsored, career development strategy session, especially designed for graduate students and young professionals, who are Graduates of the Last Decade (GOLD). The session includes a seminar on career development strategies in today's globally competitive world and a panel discussion focusing on career options and career path selection with expert panelists from academia, research, design, development and manufacturing and will be followed by a golden opportunity for you to meet with EDS Officers and Administrative Committee (AdCom) members at a special networking session. Establishing a network with successful EDS Adcom members and enjoying some of the other key EDS benefits (e.g., online access to ED Letters and Transactions and the IEDM proceedings) are some of the primary reasons for joining EDS.

Ed Jollie of IBM Corporation will present a seminar entitled **Business and Technical Leadership - an overview and discussion on things those early in their career should be aware of and consider as they map their future goals**. In his current position as Business and Technical Leadership Partner, Systems Technology Group and Integrated Supply Chain at IBM, Ed is responsible for Business and Technical Executive identification, development, and placement. His worldwide responsibilities include advising and collaborating with the Executive Management team of both units in the development of the global executive team.

For additional details on this EDS sponsored GOLD event, please contact EDS GOLD representative, Dr. Ravi Todi at rtodi@ieee.org

MEMBERSHIP PROMOTION FOR NON-IEEE MEMBERS: Conference registrants will be able to join IEEE, and the Electron Devices Society (EDS) during the conference at the IEEE Membership Desk located in the Registration Center. If you registered and paid for the conference as a non-member, you will be receiving a CREDIT voucher worth $25 towards an IEEE membership, and free EDS membership for one year (worth $12). STUDENTS

registering at the student non-member rate will receive a credit voucher that will entitle them to one-year of FREE IEEE and EDS memberships.

MEMBERSHIP PROMOTION FOR CURRENT IEEE MEMBERS: FREE Electron Devices Society membership for one-year will be offered to any IEEE member attending the IEDM who is not currently a member of EDS. A FREE EDS Membership Credit Voucher will be available at the IEEE Membership Desk. Just complete the voucher by providing your name, address and member number and submit it at the Membership Desk. If you are currently a member of EDS, you cannot use this voucher to renew your membership. Credit vouchers are only valid at the IEDM and must be redeemed at the IEEE Membership Desk. Copies of the 2010 EDS Membership Brochure are also available at the Membership Desk, which will be open the following hours:

Monday, December 7, 9:00 a.m. - 5:00 p.m.
Tuesday, December 8, 9:00 a.m. - 5:00 p.m.
Wednesday, December 9, 9:00 a.m. - 3:00 p.m.

MESSAGE CENTER: An IEDM Message Board will be in operation in the Registration Center during registration hours. Please advise callers who wish to reach you during the day to ask the hotel operator 443-573-8715 for the IEDM Conference Message Desk. Please check the message board periodically.

ROGER A. HAKEN BEST STUDENT PAPER: The 2008 Roger A. Haken Best Student Paper Award will be presented on Monday, December 7, at the Plenary Session to Jianqiang Lin of the National University of Singapore for the paper entitled, "Plasma PH3-Passivated High Mobility Inversion InGaAs MOSFET Fabricated with Self-Aligned Gate First Process and HfO_2/TaN Gate Stack".

One paper presented by a student at the 2009 IEDM will be selected for the 2009 Best Student Paper Award. To be eligible, the paper must be based on the student's own work and have been identified as a student paper at the time of submission. Presentation of the award will be made at the 2010 IEDM.

BADGES: Badges are required for admittance to all sessions and the Wine and Cheese Reception. Please wear your badge at all times while attending the conference, so that you will not be delayed entry to a session.

PRESS ROOM: Beginning on Monday, the Press Room will be in operation during registration hours.

To keep the quality of the presentations at a maximum, absolutely no cell phones, pagers or photos will be permitted during any of the sessions.

RECRUITING: In keeping with the long standing tradition of fostering a low key, research oriented atmosphere for the IEDM, the Conference Committee and the Electron Devices Society of the IEEE discourage overt and highly visible recruiting activities in association with the IEDM. **IEEE policy #9.18 prohibits recruiting at IEEE-sponsored conferences, consequently, recruiters and recruitment advertisements will not be permitted in IEDM hotel space or meeting facilities and all unauthorized material will be removed from the premises.**

PLEASE DIRECT CONFERENCE INQUIRIES TO:

Phyllis Mahoney
IEDM
19803 Laurel Valley Place
Montgomery Village, MD 20886 USA
TEL: 301/527-0900 ext. 103
FAX: 301/527-0994
EMAIL: iedm@his.com

Seated from left to right: Stefan DeGendt, Process Technology Subcommittee Chair; Howard C.-H. Wang, Short Course Vice Chair; Sunae Seo, Solid State and Nanoelectronic Devices Chair; Kazunari Ishimaru, Technical Program Vice Chair; Vivek Subramanian, General Chair; Meikei Ieong, Technical Program Chair; Veena Misra, Publicity Chair; Toshiro Hiramoto Emerging Technologies Chair.

Standing from left to right: Corin Ford, Conference Planner; Kiyotaka Imai, CMOS and Devices Subcommittee Chair; Tahir Ghani, Publications Chair; Frederic Boeuf, European Arrangements Chair; Norikatsu Takaura, Memory Technology Subcommittee Chair; John Suehle, Publicity Vice Chair; Werner Weber, Displays, Sensors, and MEMS Subcommittee Chair; Giovanni Ghione, European Arrangements Chair; Masami Hane, Asian Arrangements Chair; Phil Oldiges, Modeling and Simulation Subcommittee Chair; Roland Thewes, Short Course Chair; Patrick Fay, Quantum, Power, and Compound Semiconductor Devices Subcommittee Chait; Albert Chin, Asian Arrangements Chair; Tanya Nigam, Characterization, Reliability and Yield Subcommittee Chair.

Missing: Phyllis Mahoney, Conference Planner

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1.3 New Perspectives from Micro and Nanotechnologies in Healthcare and Diagnosis, Jean Chabbal, CEA, LETI, MINATEC — 7

Session 2: Process Technology - CMOS Junctions: Advanced Anneals and Metrology
Monday, December 7, 1:30 p.m.
Holiday Ballrooms 1, 2 and 3

1:35 p.m.
2.1 Silicide Yield Improvement with NiPtSi Formation by Laser Anneal for Advanced Low Power Platform CMOS Technology, C. Ortolland, E. Rosseel, N. Horiguchi, C. Kerner, S. Mertens, J. Kittl, E. Verleysen*, H. Bender, W. Vandervost*, A. Lauwers, P.P. Absil, S. Biesemans, S. Muthukrishnan**, S. Srinivasan**, A.J. Mayur**, R. Schreutelkamp**, T. Hoffmann, IMEC, *KU Leuven, **Applied Materials — 8

2:00 p.m.
2.2 A Study on Millisecond Annealing (MSA) Induced Layout Dependence for Flash Lamp Annealing (FLA) and Laser Spike Annealing (LSA) in Multiple MSA Scheme with 45nm High-Performance Technology, T. Miyashita, T. Kubo, Y.S. Kim, M. Nishikawa, Y. Tamura, J. Mitani, M. Okuno, T. Tanaka, H. Suzuki, T. Sakata, T. Kodama, T. Itakura, N. Idani, T. Mori, Y. Sambonsugi, A. Shimizu, H. Kurata, T. Futatsugi, Fujitsu Microelectronics Limited — 8

2:25 p.m.
2.3 3D 65nm CMOS with 320°C Microwave Dopant Activation, Y.-J. Lee, Y.-L. Lu*, F.-K. Hsueh, K.-C. Huang*, C.-C. Wan*, .T.-Y. Cheng*, M.-H. Han*, J.M. Kowalski**, J.E. Kowalski**, D. Heh, H.-T. Chuang, Y. Li*, T.-S. Chao*, C.-Y. Wu^, F.-L. Yang, National Nano Device Laboratories, *National Chiao Tung University, **DSG Technologies, Inc., ^Dayeh University — 9

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2.4 Insight into the S/D Engineering by High-resolution Imaging and Precise Probing of 2D-Carrier Profiles with Scanning Spreading Resistance Microscopy, L. Zhang, M. Saitoh, A. Kinoshita, N. Yasutake, A. Hokazono, N. Aoki, N. Kusunoki, I. Mizushima, M. Koike, S. Takeno, J. Koga, Toshiba Corporation — 9

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2.5 Strain Metrology of Devices by Dark-Field Electron Holography: A New Technique for Mapping 2D Strain Distributions (Invited), M. Hÿtch, F. Hüe*, F. Houdellier, E. Snoeck, A. Claverie, CEMES-CNRS, *University of Cambridge — 10

Session 3: CMOS Devices and Technology – Device Scaling and Variability
Monday, December 7, 1:30 p.m.
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1:35 p.m.
3.1 Dual Metallic Source and Drain Integration on Planar Single and Double Gate SOI CMOS Down to 20nm: Performance and Scalability Assessment, L. Hutin, M. Vinet, T. Poiroux, C. Le Royer, B. Previtali, C. Vizioz, D. Lafond, Y. Morand*, M. Rivoire*, F. Nemouchi, V. Carron, T. Billon, S. Deleonibus, O. Faynot, CEA/LETI, MINATEC, *STMicroelectronics — 10

2:00 p.m.
3.2 Extremely Thin SOI (ETSOI) CMOS with Record Low Variability for Low Power System-on-Chip Applications, K. Cheng, A. Khakifirooz, P. Kulkarni, S. Ponoth, J. Kuss, D. Shahrjerdi*, L.F. Edge, A. Kimball, S. Kanakasabapathy, K. Xiu**, S. Schmitz, A. Reznicek, T. Adam, H. He, N. Loubet***, S. Holmes, S. Mehta, D. Yang**, A. Upham, S.-C. Seo, J.L. Herman, R. Johnson, Y. Zhu*, P. Jamison, B.S. Haran, Z. Zhu**, L.H. Vanamurth, S. Fan, D. Horak, H. Bu, P.J. Oldiges**, D.K. Sadana*, P. Kozlowski, D. McHerron, J. O'Neill, B. Doris, IBM, *IBM TJ Watson Research Center, **IBM SRDC, ***STMicroelectronics — 11

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3.3 Carrier Profile Designing to Suppress Systematic V_{th} Variation Related with Device Layout by Controling STI-enhanced Dopant Diffusions Correlated with Point Defects, H. Fukutome, Y. Momiyama, A. Satoh, Y. Tamura, H. Minakata, K. Okabe, E. Mutoh, K. Suzuki, A. Usujima, H. Arimoto, S. Satoh, Fujitsu Microelectronics — 11

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3.4 Physical Model of the Impact of Metal Grain Work Function Variability on Emerging Dual Metal Gate MOSFETs and its Implication for SRAM Reliability, X. Zhang, J. Li*, M. Grubbs, M. Deal, B. Magyari-Kope, B. Clemens, Y. Nishi, Stanford University, *IBM — 12

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3.5 Experimental Investigation and Design Optimization Guidelines of Characteristic Variability in Silicon Nanowire CMOS Technology, J. Zhuge*, R. Wang*, R. Huang*, J. Zou*, X. Huang*, D.-W. Kim**, D. Park**, X. Zhang*, Y. Wang*, Peking University, *Ministry of Education, **Samsung Electronics Co. — 12

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4.4 Self-Consistent Monte Carlo Device Simulations Under Nano-Scale Device Structures: Role of Coulomb Interaction, Degeneracy, and Boundary Condition, K. Nakanishi, T. Uechi, N. Sano, University of Tsukuba — 14

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4.5 New Insight on the Charge Trapping Mechanisms of SiN-Based Memory by Atomistic Simulations and Electrical Modeling, E. Vianello, L. Perniola, P. Blaise, G. Molas, J.P. Colonna, F. Driussi*, P. Palestri*, D. Esseni*, L. Selmi*, N. Rochat, C. Licitra, D. Lafond, R. Kies, G. Reimbold, B. De Salvo, F. Boulanger, CEA-LETI MINATEC, *DIEGM — 15

Session 5: Memory Technology – PRAM and RRAM
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5.2 1D Thickness Scaling Study of Phase Change Material ($Ge_2Sb_2Te_5$) Using a Pseudo 3-Terminal Device, B.-J. Bae, S. Kim*, Y. Zhang*, Y.K. Kim, I.G. Baek, S. Park, I.-S. Yeo, S. Choi, J.-T. Moon, H.-S.P. Wong*, K. Kim, Samsung Electronics Co. Ltd., *Stanford University — 16

2:25 p.m.
5.3 Phase Change Memory Technology for Embedded Non Volatile Memory Applications for 90nm and Beyond, R. Annunziata, P. Zuliani, M. Borghi, G. De Sandre, L. Scotti, C. Prelini, M. Tosi*, I. Tortorelli*, F. Pellizzer*, STMicroelectronics, *Numonyx — 16

2:50 p.m.
5.4 Effect of Oxygen Migration and Interface Engineering on Resistance Switching Behavior of Reactive Metal/Polycrystalline $Pr_{0.7}Ca_{0.3}MnO_3$ Device for Nonvolatile Memory Applications, D.-J. Seong, J. Park, N. Lee, M. Hasan, S. Jung, H. Choi, J. Lee, M. Jo, W. Lee, S. Park, S. Kim, Y.H. Jang, Y. Lee*, M. Sung*, D. Kil*, Y. Hwang*, S. Chung*, S. Hong*, J. Roh*, H. Hwang, Gwangju Institute of Science and Technology, *Hynix Semiconductor Inc. — 17

3:15 p.m.
5.5 Highly Scalable Hafnium Oxide Memory with Improvements of Resistive Distribution and Read Disturb Immunity, Y.S. Chen*, H.Y. Lee*, P.S. Chen**, P.Y. Gu*, C.W. Chen*, W.P. Lin*, W.H. Liu*, Y.Y. Hsu*, S.S. Sheu*, P.C. Chiang*, W.S. Chen*, F.T. Chen*, C.H. Lien, M.-J. Tsai*, National Tsing Hua University, *Industrial Technology Research Institute, **MingShin University of Science and Technology, — 17

3:40 p.m.
5.6 High Density and Ultra Small Cell Size of Contact ReRAM (CR-RAM) in 90nm CMOS Logic Technology and Circuits, Y.H. Tseng, C.-E. Huang, C.-H. Kuo*, Y.-D. Chih*, C.J. Lin, National Tsing-Hua University, *TSMC — 18

4:05 p.m.
5.7 A 45nm Generation Phase Change Memory Technology, G. Servalli, Numonyx — 18

Session 6: Characterization, Reliability, and Yield–Hi-K
Monday, December 7, 1:30 p.m.
Key Ballrooms 8, 11 and 12

1:35 p.m.
6.1 Fermi Level Pinning in Si, Ge and GaAs Systems - MIGS or Defects? (Invited), J. Robertson, L. Lin, Cambridge University — 19

2:00 p.m.
6.2 Negatively Charged Deep Level Defects Generated by Yttrium and Lanthanum Incorporation into HfO_2 for V_{th} Adjustment, and the Impact on TDDB, PBTI and 1/*f* Noise, M. Sato, S. Kamiyama, Y. Sugita, T. Matsuki, T. Morooka, T. Suzuki, K. Shiraishi*, K. Yamabe*, K. Ohmori**, K. Yamada**, J. Yugami, K. Ikeda, Y. Ohji, Selete, *University of Tsukuba, **Waseda University — 19

2:25 p.m.
6.3 Impact of Dipole-Induced Dielectric Relaxation on High-frequency Performance in La-Incorporated HfSiON/Metal Gate nMOSFET, G.B. Choi, H.C. Sagong, K.T. Lee, M.S. Park, H.S. Choi, S.H. Song, R.H. Baek, C.H. Park, S.H. Lee, J.S. Lee, C.Y. Kang*, H-H. Tseng*, R. Jammy*, Y.H. Jeong, Pohang University of Science and Technology, *SEMATECH, NCNT — 20

2:50 p.m.
6.4 Reversible and Irreversible Degradation Attributing to Oxygen Vacancy in HfSiON Gate Films During Electrical Stress Application, R. Hasunuma, C. Tamura, T. Nomura, Y. Kikuchi, K. Ohmori*, M. Sato**, A. Uedono, T. Chikyow^, K. Shiraishi, K. Yamada**, K. Yamabe, University of Tsukuba, *Waseda University, **SELETE, ^NIMS — 20

3:15 p.m.
6.5 Observation of Switching Behaviors in Post-Breakdown Conduction in NiSi-gated Stacks, W.H. Liu, K.L. Pey, X. Li, M. Bosman*, Nanyang Technological University, *Institute of Microelectronics **21**

3:40 p.m.
6.6 A Discharge-Based Multi-Pulse Technique (DMP) for Probing Electron Trap Energy Distribution in High-*k* Materials for Flash Memory Application, X.F. Zheng, W.D. Zhang, B. Govoreanu*, J.F. Zhang, J. van Houdt*, Liverpool John Moores University, *IMEC **21**

Session 7: Quantum, Power, and Compound Semiconductors – Power Devices: Si, SiC, GaN
Monday, December 7, 1:30 p.m.
Key Ballrooms 3, 4 and 6

1:35 p.m.
7.1 NexFET A New Power Device, S. Xu, J. Korec, D. Jauregui, C. Kocon, S. Malloy, H. Lin, G. Daum, S. Perellia, K. Barry, C. Pearce, O. Lopez, J. Herbsommer, Texas Instruments **22**

2:00 p.m.
7.2 Power MOSFETs, IGBTs, and Thyristors in SiC: Optimization, Experimental Results, and Theoretical Performance (Invited), J.A. Cooper, T. Tamaki*, G.G. Walden, S. Sue, S.R. Wang, X. Wang, Purdue University, *Renesas Tech. Corp **22**

2:25 p.m.
7.3 A Normally-off GaN FET with High Threshold Voltage Uniformity Using A Novel Piezo Neutralization Technique, K. Ota, K. Endo, Y. Okamoto, Y. Ando, H. Miyamoto, H. Shimawaki, NEC Corporation **23**

2:50 p.m.
7.4 Low Leakage High Breakdown E-Mode GaN DHFET on Si by Selective Removal of In-Situ Grown Si_3N_4, J. Derluyn, M. Van Hove, D. Visalli, A. Lorenz, D. Marcon, P. Srivastava, K. Geens, B. Sijmus, J. Viaene, X. Kang, J. Das, F. Medjdoub, K. Cheng, S. Degroote, M. Leys, G. Borghs, M. Germain, IMEC **23**

3:15 p.m.
7.5 Normally-off 5A/1100V GaN-on-Silicon Device for High Voltage Applications, K.S. Boutros, S. Burnham, D. Wong, K. Shinohara, B. Hughes, D. Zehnder, C. McGuire, HRL Laboratories **24**

3:40 p.m.
7.6 GaN Monolithic Inverter IC Using Normally-off Gate Injection Transistors with Planar Isolation on Si Substrate, Y. Uemoto, T. Morita, A. Ikoshi, H. Umeda, H. Matsuo, J. Shimizu, M. Hikita, M. Yanagihara, T. Ueda, T. Tanaka, D. Ueda, Panasonic Corporation **24**

4:05 p.m.
7.7 Correlation Between DC and rf Degradation Due to Deep Levels in AlGaN/GaN HEMTs, A. Chini*, F. Fantini*, V. Di Lecce*, M. Esposto*, A. Stocco, N. Ronchi, F. Zanon, G. Meneghesso, E. Zanoni, University of Padova, *University of Modena and Reggio Emilia **25**

4:30 p.m.
7.8 InAlN/GaN Heterostructures for Microwave Power and Beyond (Invited), E. Kohn, M. Alomari, A. Denisenko, M. Dipalo, D. Maier, F. Medjdoub, C. Pietzka, S. Delage[1], M.-A. di Forte-Poisson[1], E. Morvan[1], N. Sarazin[1], J.-C. Jacquet[1], C. Dua[1], J.-F. Carlin[2], N. Grandjean[2], M. Py[2], M. Gonschorek[2], J. Kuzmik[3], D. Pogany[3], G. Pozzovivo[3], C. Ostermaier[3], L. Toth[4], B. Pecz[4], J.-C. De Jaeger[5], C. Gaquiere[5], K. Cico[6], K. Fröhlich[6], A. Georgakilas[7], E. Iliopoulos[7], G. Konstantinidis[7], C. Giessen[8], M. Heuken[8], B. Schineller[8], Ulm University, [1]Alcatel, [2]EPFL, [3]Technological University of Wien, [4]MFA, [5]IEMN, [6]IEE, [7]FORTH, [8]Aixtron **25**

Session 8: Displays, Sensors, and MEMS – TFT Technologies
Monday, December 7, 1:30 p.m.
Key Ballroom 5

1:35 p.m.
8.1 Integrated High Performance (100) and (110) Oriented Single-Grain Si TFTs without Seed Substrate, T. Chen, R. Ishihara, J. van der Cingel, B. Alessandro, M.R. Tajari Mofrad, H. Schellevis, K. Beenakker, Delft University of Technology **26**

2:00 p.m.
8.2 A Novel Five-Photo-Mask Low-Temperature Polycrystalline-Silicon CMOS Structure, S.-J. Lee, S.-W. Lee, K.-M. Oh, K.-E. Lee, M.-S.Yang, Y.-K. Hwang, LG Display **26**

2:25 p.m.
8.3 Integration of Single Crystal Si TFTs and Circuits on a Large Glass Substrate, Y. Takafuji, Y. Fukushima, K. Tomiyasu, M. Takei, Y. Ogawa, K. Tada, S. Matsumoto, H. Kobayashi,Y. Watanabe, E. Kobayashi, S.R. Droes*, A.T. Voutsas*, J. Hartzell*, Sharp Corporation, *Sharp Laboratories of America Inc. **27**

2:50 p.m.
8.4 High Performance Amorphous Oxide Thin Film Transistors with Self-Aligned Top-Gate Structure, J.C. Park, S.W. Kim, S.I. Kim, H. Yin, J.H. Hur, S.H. Jeon, S.H. Park, I.H. Song, Y.S. Park, U.I. Chung, M.K. Ryu, S. Lee*, S. Kim*, Y. Jeon*, D.M. Kim*, D.H. Kim* , K.-W. Kwan**, C.J. Kim, Samsung Advanced Institute of Technology, *Kookmin University, **Sungkyunkwan University **27**

3:15 p.m.
8.5 ZnO Thin Film Transistors and Circuits on Glass and Polyimide by Low-Temperature PEALD, D.A. Mourey, D.A. Zhao, T.N. Jackson, Pennsylvania State University **28**

3:40 p.m.
8.6 High Performance Low Voltage Amorphous Oxide TFT Enhancement/Depletion Inverter Through Uni-/Bi-Layer Channel Hybrid Integration, H. Yin, S. Kim, J. Park, I. Song, S.-W. Kim, J. Hur, S. Park, S. Jeon, C.J. Kim, Samsung Electronics **28**

4:05 p.m.
8.7 Novel, 100 V, Trench Super Junction High Voltage TFTs using Low Temperature Poly Crystalline Silicon, M.H. Dhyani, D. Green, M. Sweet, E.M. Sankara Narayanan, S.C. Deane*, N.D. Young*, Sheffield University, *Philips Research Laboratories **29**

4:30 p.m.
8.8 A Novel LTPS-TFT-Based Charge-Trapping Memory Device with Field-Enhanced Nanowire Structure, T.-C. Liao, S.-K. Chen, M.H. Yu, C.-Y. Wu, T.-K. Kang*, F.-T. Chien*, Y.-T. Liu, C.-M. Lin*, H.-C. Cheng, National Chiao Tung University, *Feng Chia University 29

Session 9: Solid-State and Nanoelectronics Devices – Spin Devices and Nano-Electromechanical Devices
Monday, December 7, 1:30 p.m.
Key Ballrooms 1 and 2

1:35 p.m.
9.1 Silicon Spintronics: Spin Injection, Manipu-lation and Electrical Detection (Invited), B.T. Jonker, O.M.J. van 't Erve, G. Kioseoglou, A.T. Hanbicki, C.H. Li, M. Holub, C. Awo-Affouda, P.E. Thompson, Naval Research Laboratory 30

2:00 p.m.
9.2 Read/Write Operation of Spin-Based MOSFET Using Highly Spin-Polarized Ferromagnet/MgO Tunnel Barrier for Reconfigurable Logic Devices, T. Marukame, T. Inokuchi, M. Ishikawa, H. Sugiyama, Y. Saito, Toshiba Corporation 30

2:25 p.m.
9.3 A Disturbance-Free Read Scheme and a Compact Stochastic-Spin-Dynamics-Based MTJ Circuit Model for Gb-scale SPRAM, K. Ono, T. Kawahara, R. Takemura, K. Miura, H. Yamamoto, M. Yamanouchi, J. Hayakawa, K. Ito, H. Takahashi, S. Ikeda, H. Hasegawa, H. Matsuoka, H. Ohno*, Hitachi Ltd., *Tohoku University 31

2:50 p.m.
9.4 4-Terminal Relay Technology for Complement-ary Logic, R. Nathanael, V. Pott, H. Kam, J. Jeon, T.-J. King Liu, University of California, Berkeley 31

3:15 p.m.
9.5 3-Terminal Nanoelectromechanical Switching Device in Insulating Liquid Media for Low Voltage Operation and Reliability Improvement, J.-O. Lee, M.-W. Kim, S.-D. Ko, H.-O. Kang*, W.-H. Bae*, M.-H. Kang*, K.-N. Kim*, D.-E. Yoo*, J.-B. Yoon, KAIST, *National Nanofab Center 32

Session 10: Emerging Technologies – Graphene Nano-electronics
Tuesday, December 8, 9:00 a.m.
Holiday Ballrooms 1, 2 and 3

9:05 a.m.
10.1 Graphene for VLSI: FET and Interconnect Applications (Invited), Y. Awano, Keio University 33

9:30 a.m.
10.2 Development of Graphene FETs for High Frequency Electronics (Invited), Y.-M. Lin, K. Jenkins, D. Farmer, A. Valdes-Garcia, P. Avouris, C.-Y. Sung, H.-Y. Chiu, B. Ek, IBM 33

9:55 a.m.
10.3 Graphene Nanoribbon Devices and Quantum Heterojunction Devices (Invited), P. Kim, M.Y. Han, A.F. Young, I, Meric, K.C. Shepard, Columbia University 34

10:20 a.m.
10.4 Perspectives of Graphene Nanoelectronics: Probing Technological Options with Modeling (Invited), G. Iannaccone, G. Fiore, M. Macucci, P. Michetti, M. Micheli, A. Betti, P. Marconcini, University of Pisa 34

10:45 a.m.
10.5 Spin Transport in Single – and Multi Layer Graphene (Invited), M. Shiraishi, Osaka University, PRESTO-JST 35

11:10 a.m.
10.6 NEMS Application of Graphene, C. Chen, S. Rosenblatt, K.I. Bolotini, P. Kim, I. Kymissis, H.L. Stormer, T.F. Heinz J. Hone, Columbia University H.L. Stormer, T.F. Heinz 35

Session 11: Memory Technology – RAM and Modeling of Memory Reliability
Tuesday, December 8, 9:00 a.m.
Key Ballrooms 7, 9 and 10

9:05 a.m.
11.1 Scaling Deep Trench Based eDRAM on SOI to 32nm and Beyond, G. Wang, D. Anand, N. Butt, A. Cestero, M. Chudzik, J. Ervin, S. Fang, G. Freeman, H. Ho, B. Khan, B. Kim, W. Kong, R. Krishnan, S. Krishnan, O. Kwon, J. Liu, K. McStay, E. Nelson, K. Nummy, P. Parries, J. Sim, R. Takalkar, A. Tessier, R. Todi, R. Malik, S. Stiffler, S.S. Iyer, IBM Semiconductor Research & Development Center 36

9:30 a.m.
11.2 Novel DRAM Cell with Amplified Capacitor for Embedded Application, H.-J. Cho, M.-R. Lin, GLOBALFOUNDRIES, Inc. 36

9:55 a.m.
11.3 Scalability of TiN/HfAlO/TiN MIM DRAM Capacitor to 0.7-nm-EOT and Beyond, N. Mise, O. Tonomura, T. Sekiguchi, S. Horii*, H. Itatani*, A. Ogawa*, T. Saito*, M. Sakai*, Y. Takebayashi*, H. Yamazaki*, K. Torii, Hitachi Ltd., *Hitachi Kokusai Electric Inc. 37

10:20 a.m.
11.4 RTS-like Fluctuation in Gate Induced Drain Leakage Current of Saddle-Fin Type DRAM Cell Transistor, H. Kim, K. Kim*, T.-K. Oh*, S.-Y. Cha*, S.-J. Hong*, S.-W. Park*, H. Shin, Seoul National University, Hynix Semiconuctor 37

10:45 a.m.
11.5 Atomistic Guiding Principles for MONOS-Type Memories with High Program/Erase Cycle Endurance, K. Yamaguchi, A. Otake, K. Kobayashi, K. Shiraishi, University of Tsukuba 38

11:10 a.m.
11.6 45nm Low Power CMOS Logic Compatible Embedded STT MRAM Utilizing a Reverse-Connection 1T/1MTJ Cell, C.J. Lin, S.H. Kang*, Y.J. Wang, K. Lee*, X. Zhu*, W.C. Chen*, X. Li*, W.N. Hsu*, Y.C. Kao, M.T. Liu, W.C. Chen, Y.C. Lin, M. Nowak*, N. Yu*, L. Tran, TSMC, *Qualcomm Incorporated 38

11:35 a.m.
11.7 A 0.5V Operation, 32% Lower Active Power, 42% Lower Leakage Current, Ferroelectric 6T-SRAM with V_{TH} Self-Adjusting Function for 60% Larger Static Noise Margin, S. Tanakamaru, T. Hatanaka, R. Yajima, M. Takahashi*, S. Sakai*, K. Takeuchi, University of Tokyo, *National Institute of Advanced Industrial Science and Technology 39

Session 12: CMOS Devices and Technology – FinFET and Nanowire Devices
Tuesday, December 8, 9:00 a.m.
Key Ballrooms 8, 11 and 12

9:05 a.m.
12.1 Challenges and Solutions of FinFET Integration in an SRAM Cell and a Logic Circuit for 22 nm Node and Beyond (Invited), H. Kawasaki, V.S. Basker, T. Yamashita, C.-H. Lin*, Y. Zhu*, J. Faltermeier, S. Schmitz, J. Cummings, S. Kanakasabapathy, H. Adhikari**, H. Jagannathan, A. Kumar*, K. Maitra**, J. Wang, C.-C. Yeh, C. Wang*, M. Khater*, M. Guillorn*, N. Fuller*, J. Chang*, L. Chang*, R. Muralidhar*, A. Yagishita, R. Miller**, Q. Ouyang*, Y. Zhang*, V.K. Paruchuri, H. Bu, B. Doris, M. Takayanagi, W. Haensch*, D. McHerron, J. O'Neill, K. Ishimaru, Toshiba America Electronic Components Inc. & IBM Research at Albany Nanotech, *IBM TJ Watson Research Center, **GLOBALFOUNDRIES Inc. **39**

9:30 a.m.
12.2 A 25-nm Gate-Length FinFET Transistor Module for 32nm Node, C.-Y. Chang, T.-L. Lee, C. Wann, L.-S. Lai, H.-M. Chen, C.-C. Yeh, C.-S. Chang, C.-C. Ho, J.C. Sheu, T.M. Kwok, F. Yuan, S.M. Yu, C.F. Hu, J.J. Shen, Y.H. Liu, C.P. Chen, S.-C. Chen, L.S. Chen, L. Chen, Y.H. Chiu, C.-Y. Fu, M.J. Huang, Y.-L. Huang, S. Hung, J.J. Liaw, H.C. Lin, H.H. Lin, L.-T.S. Lin, S.S. Lin, Y.J. Mii, E. Ou-Yang, M.F. Shieh, C.C. Su, S.P. Tai, H.J. Tao, M.H. Tsai, K.-T. Tseng, K.W. Wang, S.B. Wang, J.J. Xu, F.-K. Yang, S.-T. YangC.N. Yeh, TSMC **40**

9:55 a.m.
12.3 High Performance and Highly Uniform Gate-All-Around Silicon Nanowire MOSFETs with Wire Size Dependent Scaling, S. Bangsaruntip, G.M. Cohen, A. Majumdar, Y. Zhang, S.U. Engelmann, N.C.M. Fuller, L.M. Gignac, S. Mittal, J.S. Newbury, M. Guillorn, T. Barwicz, L. Sekaric, M.M. Frank, J.W. Sleight, IBM TJ Watson Research Center **40**

10:20 a.m.
12.4 Demonstration of Scaled $0.099\mu m^2$ FinFET 6T-SRAM Cell using Full-Field EUV Lithography for (Sub-)22nm Node Single-Patterning Technology, A. Veloso, S. Demuynck, M. Ercken, A.M. Goethals, S. Locorotondo, F. Lazzarino, E. Altamirano, C. Huffman, A. De Keersgieter, S. Brus, M. Demand, H. Struyf, J. De Backer, J. Hermans, C. Delvaux, B. Baudemprez, T. Vandeweyer, F. Van Roey, C. Baerts, D. Goossens, H. Dekkers, P. Ong, N. Heylen, K. Kellens, H. Volders, A. Hikavyy, C. Vrancken, M. Rakowski, S. Verhaegen, M. Dusa*, L. Romijn*, C. Pigneret*, A. Van Dijk*, R. Schreutelkamp**, A. Cockburn**, V. Gravey**, H. Meiling*, B. Hultermans*, S. Lok*, K. Shah**, R. Rajagopalan**, J. Gelatos**, O. Richard, H. Bender, G. Vandenberghe, G. P. Beyer, P. Absil, T. Hoffmann, K. Ronse, S. Biesemans, IMEC, *ASML, **Applied Materials **41**

10:45 a.m.
12.5 Experimental Assessment of Self-Heating in SOI FinFETs, A.J. Scholten, G.D.J. Smit, R.M.T. Pijper, L.F. Tiemeijer, H.P. Tuinhout, J.-L.P.J. van der Steen*, A. Mercha**[‡], M. Braccioli, D.B.M. Klaassen, NXP-TSMC Research Centre, *Universiteit Twente, **IMEC, [‡]University of Bologna **41**

11:10 a.m.
12.6 Dual Channel FinFETs as a Single High-k/Metal Gate Solution Beyond 22nm Node, C.E. Smith, H. Adhikari*, S-H. Lee, B. Coss, S. Parthasarathy, C. Young, B. Sassman, M. Cruz, C. Hobbs, P. Majhi, P.D. Kirsch, R. Jammy, SEMATECH, *GLOBAL FOUNDRIES **42**

11:35 a.m.
12.7 Relationship Between Mobility and High-k Interface Properties in Advanced Si and SiGe Nanowires, K. Tachi, M. Casse, D. Jang*, C. Dupre, A. Hubert, N. Vulliet**, C. Maffini-Alvaro, C. Vizioz, C. Carabasse, V. Delaye, J.M. Hartmann, G. Ghibaudo*, H. Iwai^, S. Cristoloveanu*, O. Faynot, T. Ernst, CEA-LETI MINATEC, *IMEP-LAHC, INPG-MINATEC, **STMicroelectronics, ^Tokyo Insitute of Technology **42**

Session 13: Quantum, Power, and Compound Semiconductors – III-V Logic Transistors with Advanced Gate Stack
Tuesday, December 8, 9:00 a.m.
Key Ballrooms 3 and 4

9:05 a.m.
13.1 Advanced High-K Gate Dielectric for High-Performance Short-Channel $In_{0.7}Ga_{0.3}As$ Quantum Well Field Effect Transistors on Silicon Substrate for Low Power Logic Applications, M. Radosavljevic, B. Chu-Kung, S. Corcoran, G. Dewey, M.K. Hudait, J.M. Fastenau*, J. Kavalieros, W.K. Liu*, D. Lubyshev*, M. Metz, K. Millard, M. Makherjee, W. Rachmady, U. Shah, R. Chau, Intel Corporation, *IQE Inc. **43**

9:30 a.m.
13.2 High-Performance Deep-Submicron Inversion-Mode InGaAs MOSFETs with Maximum G_m Exceeding 1.1 mS/µm:New HBr Pretreatment and Channel Engineering, Y.Q. Wu, M. Xu, R. Wang, O. Koybasi, P.D. Ye, Purdue University **43**

9:55 a.m.
13.3 Enabling the High-Performance InGaAs/Ge CMOS: A Common Gate Stack Solution, D. Lin, G. Brammertz, S. Sioncke, C. Fleischmann, A. Delabie, K. Martens, H. Bender, T. Conard, W.H. Tseng**, J.C. Lin**, W.E. Wang, K. Temst*, A. Vatomme*, J. Mitard, M. Caymax, M. Meuris, M. Heyns, T. Hoffmann, IMEC, *KU Leuven, **TSMC **44**

10:20 a.m.
13.4 First Experimental Demonstration of 100 nm Inversion-mode InGaAs FinFET Through Damage-Free Sidewall Etching, Y.Q. Wu, R. Wang, T. Shen, J.J. Gu, P.D. Ye, Purdue University **44**

10:45 a.m.
13.5 InGaAs MOSFET Performance and Reliability Improvement by Simultaneous Reduction of Oxide and Interface Charge in ALD (La)AlOx/ZrO_2 Gate Stack, J. Huang, N. Goel, [a]H. Zhao, C. Y. Kang, K.S. Min, G. Bersuker, [b]S. Oktyabrsky, [c]C.K. Gaspe, [c]M.B. Santos, P. Majhi, P.D. Kirsch, [d]H.-H. Tseng, [a]J.C. Lee, R. Jammy, SEMATECH, [a]University of Texas at Austin, [b]Suny-Albany, [c]University of Oklahoma, [d]Texas State University **45**

11:10 a.m.
13.6 Thermally Robust Phosphorous Nitride Interface Passivation for InGaAs Self-Aligned Gate-First n-MOSFET Integrated with High-k Dielectric, H.-J. Oh, J. Lin, S.A.B. Suleiman, G.Q. Lo*, D.L. Kwong*, D.Z. Chi**, S.J. Lee, National University of Singapore, *Institute of Microelectronics, **Institute of Materials Research and Engineering **45**

11:35 a.m.
13.7 Experimental Demonstration of 100nm Channel Length $In_{0.53}Ga_{0.47}$As-based Vertical Inter-band Tunnel Field Effect Transistors (TFETs) for Ultra Low-Power Logic and SRAM Applications (Late News), S. Mookerjea, D. Mohata, R. Krishnan, J. Singh, A. Vallett, A. Ali, T. Mayer, V. Narayanan, D. Schlom*, A. Liu** and S. Datta, The Pennsylvania State University, *Cornell University, ** IQE Inc. 46

Session 14: Process Technology – Advanced 3D Technology and Processing
Tuesday, December 8, 9:00 a.m.
Key Ballroom 6

9:05 a.m.
14.1 Advances in 3D CMOS Sequential Integration, P. Batude, M. Vinet, A. Pouydebasque, C. Le Royer, B. Previtali, C. Tabone, J.-M. Hartmann, L. Sanchez, L. Baud, V. Carron, A. Toffoli, F. Allain, V. Mazzocchi, D. Lafond, O. Thomas, O. Cueto, N. Bouzadia, D. Fleury**, A. Amara*, S. Deleonibus, O. Faynot, CEA LETI MINATEC, *ISEP, **STMicroelectronics 46

9:30 a.m.
14.2 Three-Dimensional Integration Technology Based on Reconfigured Wafer-to-Wafer and Multichip-to-Wafer Stacking Using Self-Assembly Method, T. Fukushima, E. Iwata, Y. Ohara, A. Noriki, K. Framura, K.-W. Lee, J. Bea, T. Tanaka, M. Koyanagi, Tohoku Univesity 47

9:55 a.m.
14.3 Enabling 3D-IC Foundry Technologies for 28 nm Node and Beyond: Through-Silicon-Via Integration with High Throughput Die-to-Wafer Stacking, D.Y. Chen, W.C. Chiou, M.F. Chen, T.D. Wang, K.M. Ching, H.J. Tu, W.J. Wu, C.L. Yu, K.F. Yang, H.B. Chang, M.H. Tseng, C.W. Hsiao, Y.J. Lu, H.P. Hu, Y.C. Lin, C.S. Hsu, W.S. Shue, C.H. Yu, TSMC 47

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14.5 Impact of Remnant Stress/Strain and Metal Contamination in 3D-LSIs with Through-Si Vias Fabricated by Wafer Thinning and Bonding, M. Murugesan, J.C. Bea, H. Kino, Y. Ohara, T. Kojima, A. Noriki, K.W. Lee, K. Kiyoyama, T. Fukushima, H. Nohira, T. Hattori, E. Ikenaga*, T. Tanaka, M. Koyanagi, Tohoku University, *JASRI 48

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14.6 Ultra Thinning 300-mm Wafer Down to 7-μm for 3D Wafer Integration on 45-nm Node CMOS using Strained Silicon and Cu/Low-k Interconnects, Y. S. Kim, A. Tsukune, N. Maeda*, H. Kitada*, A. Kawai**, K. Arai**, K. Fujimoto^, K. Suzuki^, Y. Mizushima^^, T. Nakamura^^, T. Ohba*, T. Futatsugi, M. Miyajima, Fujitsu Microelectronics Limited, *University of Tokyo, **DISCO Corporation, ^Dai Nippon Printing, ^^Fujitsu Laboratories Ltd. 49

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16.2 Impact of Transistor Reliability on RF Oscillator Phase Noise Degradation, V. Reddy, N. Barton, S. Martin, C. M. Hung, A. Krishnan, C. Chancellor, S. Sundar, A. Tsao, D. Corum, N. Yanduru, S. Madhavi, S. Akhtar, N. Pathak, P. Srinivasan, S. Shichijo, K. Benaissa, A. Roy, T. Chatterjee, R. Taylor, J. Krick, Brighton, J. Ondrusek, D. Barry, S. Krishnan, Texas Instruments 53

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16.3 Technologies to Further Reduce Soft Error Susceptibility in SOI, P. Oldiges, R. Dennard*, D. Heidel*, T. Ning*, K. Rodbell*, H. Tang*, M. Gordon*, L. Wissel, IBM Corporation, *IBM Research 53

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16.6 Filament Study of STI Type Drain Extended NMOS Device using Transient Interferometric Mapping, M. Shrivastava, S. Bychikhin*, D. Pogany*, J. Schneider**, M.S. Baghini, H. Gossner**, E. Gornik*, V.R. Rao, Indian Institute of Technology-Bombay, *Vienna University of Technology, **Infineon Technologies AG — 55

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16.7 Successful Suppression of Dielectric Relaxation Inherent to High-k NAND from Both Architecture and Material Points of View (Late News), J. Fujiki, N. Yasuda, R. Fujitsuka, W. Sakamoto and K. Muraoka, Toshiba Corporation

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17.1 Understanding Mobility Mechanisms in Extremely Scaled HfO_2 (EOT 0.42 nm) Using Remote Interfacial Layer Scavenging Technique and V_t-tuning Dipoles with Gate-First Process, T. Ando, M.M. Frank, K. Choi*, C. Choi, J. Bruley, M. Hopstaken, M. Copel, E. Cartier, A. Kerber*, A. Callegari, D. Lacey, S. Brown, Q. Yang, V. Narayanan, IBM TJ Watson Research Center, *GLOBALFOUNDRIES — 55

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17.2 Ti-capping Technique as a Breakthrough for Achieving Low Threshold Voltage, High Mobility, and High Reliability of pMOSFET with Metal Gate and High-k Dielectrics Technologies, H. Takahashi, H. Minakata, Y. Morisaki, S. Xiao, M. Nakabayashi, K. Nishigaya, T. Sakoda, K. Ikeda, H. Morioka, N. Tamura, M. Kase, Y. Nara, Fujitsu Microelectronics Ltd. — 56

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17.3 V_{th} Fluctuation Suppression and High Performance of HfSiON/Metal Gate Stacks by Controlling Capping-Y_2O_3 Layers for 22nm Bulk Devices, S. Kamiyama, E. Kurosawa, S. Abe, M. Kitajima, T. Aminaka, T. Aoyama, K. Ikeda, Y. Ohji, Selete — 56

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17.5 Engineering the Complete MANOS-type NVM Stack for Best in Class Retention Performance, D.C. Gilmer, N. Goel, H. Park, C. Park, S. Verma*, G. Bersuker, P. Lysaght, H.-H. Tseng**, P.D. Kirsch, K.C. Saraswat, R. Jammy, SEMATECH, *Stanford University, **Texas State University — 57

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18.2 Design Challenges for 22nm CMOS and Beyond” (Invited), S. Borkar, Intel — 58

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18.3 Analog and RF Design Issues in High-k and Multi-Gate CMOS Technologies (Invited), M. Fulde, D. Schmitt-Landsiedel* and G. Knoblinger, *Technical University Munich, Infineon — 59

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18.4 Design Issues and Possible Solutions for Low-Cost and High-Efficiency LSIs (Invited), M. Mizuno, NEC Electronics Corp. — 59

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18.6 Co-optimizing Process Development, Layout and Circuit Design for Cost-Effective 22nm Technology Platform (Invited), K. Michaels, PDF Solutions — 60

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19.1 Experimental Demonstration of High Mobility Ge NMOS, D. Kuzum, T. Krishnamohan*, A. Nainani, Y. Sun, P.A. Pianetta, H.S-.P. Wong, K.C. Saraswat, Stanford University, *also with Intel — 61

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19.2 Record-high Electron Mobility in Ge n-MOSFETs Exceeding Si Universality, C.H. Lee, T. Nishimura* N. Saido, K. Nagashio*, K. Kita*, A. Toriumi*, The University of Tokyo, *also with JST-CREST — 61

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19.3 Germanium for Advanced CMOS Anno 2009: A SWOT Analysis (Invited), M. Caymax, G. Eneman, F. Bellenger, C. Merckling, A. Delabie, G. Wang, R. Loo, E. Simoen, J. Mitard, B. De Jaeger, G. Hellings, K. De Meyer, M. Meuris, M. Heyns, IMEC, also K.U. Leuven, FWO-Vlaanderen, MTM, IWT-Vlaanderen — 62

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20.1 30 nm $In_{0.7}Ga_{0.3}As$ Inverted-Type HEMTs with Reduced Gate Leakage Current for Logic Applications, T.-W. Kim, D.-H. Kim, J.A. del Alamo, Massachusetts Institute of Technology **64**

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20.2 Logic Performance Evaluation and Transport Physics of Schottky-Gate III-V Compound Semi-conductor Quantum Well Field Effect Transistors for Power Supply Voltages (V_{CC}) Ranging from 0.5V to 1.0V, G. Dewey, R. Kotlyar, R. Pillarisetty, M. Radosavljeric, T. Rakshit, H. Then, R. Chau, Intel Corporation **65**

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20.3 Performance Analysis of Ultra-Scaled InAs HEMTs, N. Kharche, G. Klimeck, D.-H. Kim*, J.A. del Alamo**, M. Luisier, Purdue University, *Teledyne Scientific & Imaging LLC, **Massachusetts Institute of Technology **65**

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20.5 N-polar GaN-based Highly Scaled Self-aligned MIS-HEMTs With State-of-the-art $f_T.L_G$ Product of 16.8 GHz-μm (Late News), Nidhi, S. Dasgupta, D.F. Brown, S. Keller, J.S. Speck and U.K. Mishra, University of California Santa Barbara **66**

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21.2 Benchmarking the Device Performance at Sub 22nm Node Technologies using an SoC Framework, M. Shrivastava, B. Verma, M.S. Baghini, C. Russ*, D.K. Sharma, H. Gossner*, V.R. Rao, Indian Institute of Technology-Bombay, *Infineon Technologies **67**

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21.3 Nonlinear Dynamics Approach in Modeling of the On-State-Spreading - Related Voltage and Current Transients in 90nm CMOS Silicon Controlled Rectifiers, D. Pogany, D. Johnsson*, S. Bychikhin, K. Esmark*, P. Rodin**, E. Gornik, M. Stecher*, H. Gossner*, Vienna University of Technology, *Infineon Technologies, **Ioffe Physicotechnical Institute **68**

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21.6 Compact AC Modeling and Analysis of Cu, W, and CNT Based Through-Silicon Vias (TSVs) in 3-D ICs, C. Xu, H. Li, R. Suaya*, K. Banerjee, University of California, Santa Barbara, *Mentor Graphics Corporation **69**

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22.2 3D Heterogeneous Opto-Electronic Integration Technology for System-on-Silicon (SOS), K.-W. Lee, A. Noriki, K. Kiyoyama, S. Kanno, R. Kobayashi, W.-C. Jeong, J.-C. Bea, T. Fukushima, T. Tanaka, M. Koyanagi, Tohoku University **70**

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23.2 Metal/Graphene Contact as a Performance Killer of Ultra-high Mobility Graphene - Analysis of Intrinsic Mobility and Contact Resistance -, K. Nagashio, T. Nishimura, K. Kita, A. Toriumi, The University of Tokyo ... 74

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23.3 Silicon Photonics Technologies for Monolithic Electronic-Photonic Integrated Circuit (EPIC) Applications: Current Progress and Future Outlook (Invited), K.-W. Ang, T.-Y. Liow, Q. Fang, M.B. Yu, F.F. Ren, J. Zhang, J.W. Ng, J.F. Song, Y.Z. Xiong, G.Q. Lo, D.-L. Kwong, Institute of Microelectronics ... 75

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27.1 A Stackable Cross Point Phase Change Memory, D.C. Kau, S. Tang*, I.V. Karpov, R. Dodge*, B. Klehn, J.A. Kalb, J. Strand*, A. Diaz*, N. Leung, J. Wu*, S. Lee, T. Langtry*, K.-W. Chang, C. Papagianni*, J. Lee, J. Hirst*, H. Castro*, S. Erra, E. Flores*, N. Righos, H. Castro*, G. Spadini, Intel Corp., *Numonyx B.V. **82**

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28.1 A 32nm SoC Platform Technology with 2nd Generation High-k/Metal Gate Transistors Optimized for Ultra Low Power, High Performance, and High Density Product Applications, C.-H. Jan, M. Agostinelli, M. Buehler, Z.-P. Chen, S.-J. Choi, G. Curello, H. Deshpande, S. Gannavaram, W. Hafez, U. Jalan, M. Kang, P. Kolar, K. Komeyli, B. Landau, A. Lake, N. Lazo, S.-H. Lee, T. Leo, J. Lin, N. Lindert, S. Ma, L. McGill, C. Meining, A. Paliwal, J. Park, K. Phoa, I. Post, N. Pradhan, M. Prince, A. Rahman, J. Rizk, L. Rockford, G. Sacks, A. Schmitz, H. Tashiro, C. Tsai, P. Vandervoorn, J. Xu, L. Yang, J.-Y. Yeh, J. Yip, I. Young, K. Zhang, Y. Zhang, P. Bai, Intel Corporation **85**

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28.2 Competitive and Cost Effective High-k based 28nm CMOS Technology for Low Power Applications, F. Arnaud[1], A.Thean[2], M. Eller[3], M. Lipinski[3], Y.W. Teh[4], M. Ostermayr[3], K. Kang[6], N.S. Kim[4], K. Ohuchi[7], J-P. Han[3], D.R. Nair[2], J. Lian[3], S. Uchimura[7], S. Kohler[1], S. Miyaki[8], P. Ferreira[1], R. J.-H. Park, M. Hamaguchi, K. Miyashita, Augur[5], Q. Zhang[2], K. Strahrenberg, S. ElGhouli[1], J. Bonnouvrier[1], F. Matsuoka[7], R. Lindsay[3], J. Sudijono[4], F.S. Johnson[5], J.H. Ku[6], M. Sekine[8], A. Steegen[2], R. Sampson[1], IBM SRDC, [1]STMicroelectronics, [2]IBM Microelectronics, [3]Infineon Technologies, [4]Chartered Semiconductor Manufacturing, [5]GlobalFoundries, [6]Samsung Electronics, [7]Toshiba, [8]NEC-EL **86**

9:55 a.m.
28.3 A Novel "Hybrid" High-k/Metal Gate Process For 28nm High Performance CMOSFETs, C.M. Lai, C.T. Lin, L.W. Cheng, C.H. Hsu, J.T. Tseng, T.F. Chiang, C.H. Chou, Y.W. Chen, C.H. Yu, S.H. Hsu, C.G. Chen, Z.C. Lee, J.F Lin, C.L. Yang, G.H. Ma, S.C. Chien, United Microelectronics Corporation **86**

10:20 a.m.
28.4 High Performance 32nm Logic Technology Featuring 2nd Generation High-k + Metal Gate Transistors, P. Packan, S. Akbar, M. Armstrong, D. Bergstrom, M. Brazier, H. Deshpande, K. Dev, G. Ding, T. Ghani, O. Golonzka, W. Han, J. He, R. Heussner, R. James, J. Jopling, C. Kenyon, S-H. Lee, M. Liu, S. Lodha, B. Mattis, A. Murthy, L. Neiberg, J. Neirynck, S. Pae, C. Parker, L. Pipes, J. Sebastian, J. Seiple, B. Sell, A. Sharma, S. Sivakumar, B. Song, A. St. Amour, K. Tone, T. Troeger, C. Weber, K. Zhang, Y. Luo, S. Natarajan, Intel Corporation **87**

10:45 a.m.
28.5 Ultra Low-EOT (5 Å) Gate-First and Gate-Last High Performance CMOS Achieved by Gate-Electrode Optimization, L.-Å. Ragnarsson, Z. Li, J. Tseng, T. Schram, E. Rohr, M.J. Cho, T. Kauerauf, T. Conard, Y. Okuno, B. Parvais, P. Absil, S. Biesemans, T.Y. Hoffmann, IMEC **87**

11:10 a.m.
28.6 Hybrid FDSOI/Bulk high-k/Metal Gate Platform for Low Power (LP) Multimedia Technology, C. Fenouillet-Beranger*, P. Perreau*, L. Pham-Nguyen, S. Denorme, F. Andrieu*, L. Tosti*, L. Brevard*, O. Weber*, S. Barnola*, T. Salvetat*, X. Garros*, M. Casse*, C. Leroux*, J.P. Noel*, O. Thomas*, B. Le-Gratiet, F. Baron, M. Gattefait, Y. Campidelli, F. Abbate, C. Perrot, C. de-Buttet*, R. Beneyton, L. Pinzelli, F. Leverd, P. Gouraud, M. Gros-Jean, A. Bajolet, C. Mezzomo, C. Leyris, S. Haendler, D. Noblet, R. Pantel, A. Margain, C. Borowiak, E. Josse, N. Planes, D. Delprat^, F. Boedt^, K. Bourdelle^, B.Y. Nguyen^**, F. Boeuf, O. Faynot*, T.Skotnicki, STMicroelectronics, *CEA-LETI MINATEC, **also IMEP, MINATEC, ^SOITEC 88

11:40 a.m.
28.7 16nm Functional 0.039mm^2 6T-SRAM Cell with Nano Injection Lithography, Nanowire Channel, and Full TiN Gate (Late News), H.-Y. Chen, C.-C. Chen, F.-K. Hsueh, J.-T. Liu, C.-Y. Shen, C.-C. Hsu, S.-L. Shy, B.-T. Lin, H.-T. Chuang, C.-S. Wu, C. Hu*, C.-C. Huang, and F.-L. Yang, National Nano Device Laboratories, *University of California, Berkeley 88

11:55 a.m.
28.8 Trigate 6T SRAM Scaling to 0.06 μm^2 (Late News), M. Guillorn, J. Chang, A. Pyzyna, S. Engelmann, E. Joseph, B. Fletcher, C. Cabral, Jr., C.-H. Lin, A. Bryant, M. Darnon, J. Ott, C. Lavoie, M. Frank, L. Gignac, J. Newbury, C. Wang, D. Klaus, E. Kratschmer, J. Bucchignano, B. To, W. Graham, I. Lauer, E. Sikorski, S. Carter, V. Narayanan, N. Fuller, Y. Zhang and W. Haensch, IBM T.J. Watson Research Center 89

Session 29: Process Technology – Si Channel Engineering and Ge Technologies
Wednesday, December 9, 9:00 a.m.
Key Ballrooms 3, 4 and 6

9:05 a.m.
29.1 Steep Channel Profiles in n/pMOS Controlled by Boron-doped Si:C Layers for Continual Bulk-CMOS Scaling, A. Hokazono, H. Itokawa, I. Mizushima, S. Kawanaka, S. Inaba, Y. Toyoshima, Toshiba Corporation 89

9:30 a.m.
29.2 First CMOS Integration of Ultra Thin Body and BOX (UTB^2) Structures on Bulk Direct Silicon Bonded (DSB) Wafer with Multi-Surface Orientations, G. Bidal[1], F. Boeuf[1], S. Denorme[1], C. Laviron[3], K. Bourdelle[4], N. Loubet[1], Y. Campidelli[1], R. Beneyton[1], H. Moriceau[3], F. Fournel[3], P. Morin[1], S. Barnola[3] , T. Salvetat[3], P. Perreau[3], P. Gouraud[1], F. Leverd[1], B. Le-Gratiet[1], J.L. Huguenin[1], D. Fleury[1], K. Kusiaku[1], A. Cros[1], C. Leyris[1], S. Haendler[1], C. Borowiak[1], L. Clement[1], R. Pantel[1], G. Ghibaudo[2], T. Skotnicki[1], [1]STMicroelectronics, [2]IMEP-LAHC, [3]CEA-LETI , [4]SOITEC 90

9:55 a.m.
29.3 High Performance GeO_2/Ge nMOSFETs with Source/Drain Junctions Formed by Gas Phase Doping, K. Morii, T. Iwasaki, R. Nakane, M. Takenaka*, S. Takagi, The University of Tokyo, *also with JST-PRESTO 90

10:20 a.m.
29.4 High Performance n-MOSFETs with Novel Source/Drain on Selectively Grown Ge on Si for Monolithic Integration, H.-Y. Yu, M. Kobayashi, W.S. Jung, A.K. Okyay*, Y. Nishi, K.C. Saraswat, Stanford University, *Bilkent University 91

10:45 a.m.
29.5 A Comprehensive Study of $Ge_{1-x}Si_x$ on Ge for the Ge nMOSFETs with Tensile Stress, Shallow Junctions and Reduced Leakage, G.-L. Luo, S.-C. Huang, C.-T. Chung*, D. Heh, C.-H. Chien, C.-C. Cheng*, Y.-J. Lee, W.-F. Wu, C.-C. Hsu, M.-L. Kuo, J.-Y. Yao, M.-N. Chang, C.-W. Liu, C, Hu, C.-Y. Chang*, F.-L. Yang, National Nano Device Laboratories, *National Chiao-Tung University, National Taiwan University, University of California 91

11:10 a.m.
29.6 Comprehensive Study of GeO_2 Oxidation, GeO Desorption and GeO_2-Metal Interaction – Understanding of Ge Processing Kinetics for Perfect Interface Control-, K. Kita*, S.K. Wang, M. Yoshida, C.H. Lee, K. Nagashio*, T. Nishimura*, A. Toriumi*, The University of Tokyo, *also with JST-CREST 92

Session 30: Modeling and Simulation – Noise and Fluctuations
Wednesday, December 9, 9:00 a.m.
Key Ballroom 5

9:05 a.m.
30.1 Compact Model for Layout Dependent Variability (Invited), H. Aikawa, T. Sanuki, A. Sakata, E. Morifuji, H. Yoshimura, T. Asami, H. Otani, H. Oyamatsu, Toshiba Corporation Semiconductor Company 92

9:30 a.m.
30.2 Statistical Enhancement of Combined Simulations of RDD and LER Variability: What Can Simulation of a 10^5 Sample Teach Us?, D. Reid, C. Millar, G. Roy, S. Roy, A. Asenov, University of Glasgow 93

9:55 a.m.
30.3 Design Space and Scalability Exploration of 1T-1STT MTJ Memory Arrays in the Presence of Variability and Disturbances, A. Raychowdhury, D. Somasekhar, T. Karnik, V. De, Intel Corporation 93

10:20 a.m.
30.4 Impact of Interface States on MOS Transistor Mismatch, P. Andricciola, H.P. Tuinhout, B. De Vries, N.A.H. Wils, A.J. Scholten, D.B.M. Klaassen, NXP Semiconductor 94

10:45 a.m.
30.5 Statistical Model for MOSFET Low-Frequency Noise under Cyclo-Stationary Conditions, G. Wirth, R. da Silva P. Srinivasan*, J. Krick*, R. Brederlow*, UFRGS, *Texas Instruments 94

11:10 a.m.
30.6 Compact Modeling of Flicker Noise Variability in Small Size MOSFETs, T.H. Morshed, M.V. Dunga, J. Zhang, D.D. Lu, A.M. Niknejad, C. Hu, University of California, Berkeley 95

11:35 a.m.
30.7 Distributed-Poole-Frenkel Modeling of Anomalous Resistance Scaling and Fluctuations in Phase-Change Memory (PCM) Devices, D. Fugazza, D. Ielmini, S. Lavizzari, A.L. Lacaita, Politecnico di Milano 95

Session 31: Characterization, Reliability and Yield – BTI and Memory
Wednesday, December 9, 9:00 a.m.
Key Ballroom 1 and 2

9:05 a.m.
31.1 Switching Oxide Traps as the Missing Link Between Negative Bias Temperature Instability and Random Telegraph Noise, T. Grasser, H. Reisinger*, W. Goes, T. Aichinger**, P. Hehenberger^, P.-J. Wagner, M. Nelhiebel*, J. Franco^, B. Kaczer^, TU Wien, *Infineon, **KAI, ^IMEC **96**

9:30 a.m.
31.2 On the Differences Between Ultra-fast NBTI Measurements and Reaction-Diffusion Theory, A.E. Islam, S. Mahapatra*, S. Deora*, V.D. Maheta*, M.A. Alam, Purdue University, *IIT Bombay **96**

9:55 a.m.
31.3 Can the Reaction-Diffusion Model Explain Generation and Recovery of Interface States Contributing to NBTI?, Z. Teo, D.S. Ang, K.S. See*, Nanyang Technological University, *Chartered Semiconductor Manufacturing **97**

10:20 a.m.
31.4 New Degradation Mechanisms and Reliability Performance in Tunneling Field Effect Transistors, G.F. Jiao, Z.X. Chen**, H.Y. Yu**, X.Y. Huang, D.M. Huang, N. Singh*, G.Q. Lo*, D.-L. Kwong*, M.-F. Li, Fudan University, *Institute of Microelectronics, **also with Nanyang Technological University **97**

10:45 a.m.
31.5 Reliability of Barrier Engineered Charge Trapping Devices for Sub-30nm NAND Flash (Invited), R. Liu, H.-T. Lue, K.C. Chen, C.-Y. Lu, Macronix Int'l Co. Ltd. **98**

11:10 a.m.
31.6 Resolving Fast V_{TH} Transients After Program/Erase of Flash Memory Stacks and Their Relation to Electron and Hole Defects, M. Toledano-Luque, R. Degraeve*, M.B. Zahid*, B. Kaczer*, J. Kittl*, M. Jurczak*, G. Groeseneken*, J. Van Houdt*, Universidad Complutense de Madrid, *IMEC **98**

11:35 a.m.
31.7 Understanding Amorphous States of Phase-Change Memory Using Frenkel-Poole Model, Y.H. Shih, M.H. Lee, M. Breitwisch*, R. Cheek*, J.Y. Wu, B. Rajendran*, Y. Zhu*, E.K. Lai, C.F. Chen, H.Y. Cheng, A. Schrott*, E. Joseph*, R. Dasaka*, S. Raoux*, H.L. Lung, C. Lam*, Macronix International Co. Ltd., *IBM TJ Watson Research Center **99**

Session 32: Characterization, Reliability and Yield – Random Telegraph Noise
Wednesday, December 9, 1:30 p.m.
Holiday Ballrooms 1, 2 and 3

1:35 p.m.
32.1 New Analysis Methods for Comprehensive Understanding of Random Telegraph Noise, T. Nagumo, K. Takeuchi, S. Yokogawa, K. Imai, Y. Hayashi, NEC Electronics Corporation **99**

2:00 p.m.
32.2 Characterization of Oxide Traps Leading to RTN in High-k and Metal Gate MOSFETs, S. Lee, H.-J. Cho, Y. Son, D.S. Lee, H. Shin, Seoul National University **100**

2:25 p.m.
32.3 Impact of Random Telegraph Signals on V_{min} in 45nm SRAM, S.O. Toh, Y. Tsukamoto*, Z. Guo, L. Jones, T.-J. King Liu, B. Nikolic, University of California, Berkeley, *Renesas Technology Corp. **100**

2:50 p.m.
32.4 Reduction of Random Telegraph Noise in High-*k*/Metal-gate Stacks for 22 nm Generation FETs, N. Tega, H. Miki, Z. Ren***, C.P. D'Emic**, Y. Zhu**, D.J. Frank**, J. Cai**, M.A. Guillorn**, D.-G. Park**, W. Haensch**, K. Torii*, Hitachi America Ltd., *Hitachi Ltd., **IBM TJ Watson Research Center, ***IBM SRDC **101**

3:15 p.m.
32.5 Effect of Bottom Electrode of ReRAM with Ta_2O_5/TiO_2 Stack on RTN and Retention, M. Terai, Y. Sakotsubo, Y. Saito, S. Kotsuji, H. Hada, NEC Corporation **101**

3:40 p.m.
32.6 A New and Simple Experimental Approach to Characterizing the Carrier Transport and Reliability of Strained CMOS Devices in the Quasi-Ballistic Regime, E.R. Hsieh, S.S. Chung, P.W. Liu*, W.T. Chiang*, C.H. Tsai*, W.Y. Teng*, C.I. Li*, T.F. Kuo*, Y.R. Wang*, C.L. Yang*, C.T. Tsai*, G.H. Ma*, National Chiao Tung University, *United Microelectronics Corporation **102**

Session 33: Displays, Sensors and MEMS – Micro-Resonators and RF MEMS
Wednesday, December 9, 1:30 p.m.
Holiday Ballroom 6

1:35 p.m.
33.1 Temperature Compensated Solidly Mounted Bulk Acoustic Wave Resonators with Optimum Piezoelectric Coupling Coefficient, M.A. Allah, J. Kaitila*, R. Thalhammer*, W. Weber*, D. Schmitt-Landsiedel, Technical University of Munich, *Infineon Technologies AG **102**

2:00 p.m.
33.2 Temperature Compensation of Silicon Micromechanical Resonators via Degenerate Doping, A.K. Samarao, F. Ayazi, Georgia Institute of Technology **103**

2:25 p.m.
33.3 Self-Sustained Low Power Oscillator Based on Vibrating Body Field Effect Transistor, D. Grogg, S. Ayoz, A.M. Ionescu, Ecole Polytechnique Fédérale de Lausanne **103**

2:50 p.m.
33.4 BEOL Embedded RF-MEMS Switch for mm-Wave Applications, M. Kaynak, K.E. Ehwald, J. Drews, R. Scholz, F. Korndorfer, D. Knoll, B. Tillack, R. Barth, M. Birkholz, K. Schulz, Y.M. Sun, D. Wolansky, S. Leidich*, S. Kurth*, Y. Gurbuz**, IHP, *Fraunhofer Research Institution for Electronic Nano Systems, **Sabanci University Orhanli **104**

3:15 p.m.
33.5 Low-Loss MEMS Band-Pan Filters with Improved Out-of-Band Rejection by Exploiting Inductive Parasitics, Y. Shim, R. Tabrizian*, F. Ayazi*, M. Rais-Zadeh, University of Michigan, Ann Arbor, *Georgia Institute of Technology **104**

3:40 p.m.
33.6 Highly Tunable Band-Stop Filters Based on AlN RF MEM Capacitive Switches with Inductive Arms and Zipping Capacitive Coupling, M. Fernandez-Bolanos, T. Lisec*, C. Dehollain, D. Tsamados, P. Nicole**, A.M. Ionescu, Ecole Polytechnique Fédérale de Lausanne, *Fraunhofer-Institut fur Siliziumtechnologie, **THALES Airborne Systems **105**

4:05 p.m.
33.7 Design and Reliability of a Micro-Relay Technology for Zero-Standby-Power Digital Logic Applications, H. Kam, V. Pott, R. Nathanael, J. Jeon, E. Alon, T.-J. King Liu, University of California, Berkeley **105**

4:30 p.m.
33.8 Body-Biased Complementary Logic Implemented Using AlN Piezoelectric MEMS Switches, N. Sinha, T. Jones, Z. Guo, G. Piazza, University of Pennsylvania **106**

Session 34: Memory Technology – Flash Memory
Wednesday, December 9, 1:30 p.m.
Key Ballrooms 7, 9 and 10

1:35 p.m.
34.1 Investigation of Ballistic Current in Scaled Floating-Gate NAND FLASH and a Solution, S. Raghunathan, T. Krishnamohan, K. Parat*, K. Saraswat, Stanford University, *Intel Corp. **106**

2:00 p.m.
34.2 The New Program/Erase Cycling Degradation Mechanism of NAND Flash Memory Devices, A. Fayrushin, K.S.Seol, J.H. Na, S.H. Hur, J.D. Choi, K. Kim, Samsung Electronics **107**

2:25 p.m.
34.3 A Novel Planar Floating-Gate (FG) / Charge-Trapping (CT) NAND Device Using BE-SONOS Inter-Poly Dielectric (IPD), H.-T. Lue, P.-Y. Du, T.-H. Hsu, Y.-H. Hsiao, S.-C. Lai, S.-Y. Wang, S.P. Hong, M.T. Wu, F.H. Hsu, N.Z. Lien, C.-P. Lu, J.-Y. Hsieh, L.-W. Yang, T. Yang, K.-C. Chen, K.-Y. Hsieh, R. Liu, C.-Y. Lu, Macronix International Co. Ltd. **107**

2:50 p.m.
34.4 Reliability Improvement in Planar MONOS Cell for 20nm-node Multi-Level NAND Flash Memory and Beyond, W. Sakamoto, T. Yaegashi, T. Okamura, T. Toba, K. Komiya, K. Sakuma, Y. Matsunaga, Y. Ishibashi, H. Nagashima, M. Sugi, N. Kawada, M. Umemura, M. Kondo, T. Izumida, N. Aoki, T. Watanabe, Toshiba Corporation **108**

3:15 p.m.
34.5 Potential Well Engineering by Partial Oxidation of TiN for High-Speed and Low-Voltage Flash Memory with Good 125°C Data Retention and Excellent Endurance, G. Zhang*, C.H. Ra*, H.-M. Li, C. Yang, W.J. Yoo, Sungkyunkwan University, *also with Korea Institute of Science and Technology **108**

3:40 p.m.
34.6 Understanding STI Edge Fringing Field Effect on the Scaling of Charge-Trapping (CT) NAND Flash and Modeling of Incremental Step Pulse Programming (ISPP), H.-T. Lue, T.-H. Hsu, Y.-H. Hsiao, S.-C. Lai, E.-K. Lai, S.-P. Hong, M.-T. Wu, F.-H. Hsu, N.Z. Lien, C.-P. Lu, S.-Y. Wang, J.-Y. Hsieh, L.-W. Yang, T. Yang, K.-C. Chen, K.-Y. Hsieh, R. Liu, C.-Y. Lu, Macronix International Co. Ltd. **109**

4:05 p.m.
34.7 Program Charge Effect on Random Telegraph Noise Amplitude and Its Device Structural Dependence in SONOS Flash Memory, J.P. Chiu, Y.L. Chou, H.C. Ma, T. Wang, S.H. Ku*, N.K. Zou*, V. Chen*, W.P. Lu*, K.C. Chen*, C.-Y. Lu*, National Chiao-Tung University, *Macronix International Co. Ltd. **109**

Session 35: Quantum, Power and Compound Semiconductors – CMOS Compatible, High Mobility III-V Devices
Wednesday, December 9, 1:30 p.m.
Key Ballrooms 8, 11 and 12

1:35 p.m
35.1 High-Performance InSb Based Quantum Well Field Effect Transistors for Low-Power Dissipation Applications (Invited), T. Ashley, M. Emeny, D. Hayes, K. Hilton, R. Jefferies, J. Maclean, S.Smith, A. Tang, D. Wallis and P. Weber, QintiQ **110**

2:00 p.m.
35.2 Monolithic Integration of InSb Hall-Effect Devices with Si LSI on Si Substrate, Y. Kunimi, A. Sakurai, S. Akiyama, H. Fujita, Y. Shibata, K. Nagakura, Y. Noma, T. Yamamoto, Y. Yamaha, Asahi-KASEI Microdevices Corporation **110**

2:25 p.m.
35.3 Engineering of Strained III-V Heterostructures for High Hole Mobility, A. Nainani, S. Raghunathan, D.Witte, M. Kobayashi, T. Irisawa, T. Krishnamohan*, K. Saraswat, B.R. Bennett**, M. Ancona**, J.B. Boos**, Stanford University, *Intel Corp., **Naval Research Lab **111**

2:50 p.m.
35.4 Extraction of Virtual-Source Injection Velocity in Sub-100 nm III-V HFETs, D.-H. Kim, J.A del Alamo, D.A. Antoniadis, B. Brar*, Massachusetts Institute of Technology, *TSC **112**

3:15 p.m.
35.5 New Insight into Fermi-Level Unpinning on GaAs: Impacts of Different Surface Orientations, M. Xu, K. Xu, R. Contreras*, M. Milojevic*, T. Shen, O. Koybasi, Y.Q. Wu, R.M. Wallace*, P.D. Ye, Purdue University, *University of Texas at Dallas **112**

Session 36: Process Technology – Advanced Interconnect Technologies for CMOS Applications
Wednesday, December 9, 1:30 p.m.
Key Ballrooms 3, 4 and 6

1:35 p.m.
36.1 Optimization of Metallization Processes for 32-nm-node Highly Reliable Ultralow-k (k=2.4)/Cu Multilevel Interconnects Incorporating a Bilayer Low-k Barrier Cap (k=3.9), M. Iguchi, S. Yokogawa, H. Aizawa, Y. Kakuhara, H. Tsuchiya, N. Okada, K. Imai, M. Tohara*, K. Fujii*, T. Watanabe*, NEC Electronics Corporation, *Toshiba Corporation **112**

2:00 p.m.
36.2 Feasibility Study of 70nm Pitch Cu/Porous Low-k D/D Integration Featuring EUV Lithography Toward 22nm Generation, N. Nakamura, N. Oda, E. Soda, N. Hosoi, A Gawase, H. Aoyama, Y. Tanaka, D. Kawamura, S. Chikaki, M. Shiohara, N. Tarumi, S. Kondo, I. Mori, S. Saito, SELETE **113**

2:25 p.m.
36.3 Top-Gated FETs/Inverters with Diblock Copolymer Self-Assembled 20 nm Contact Holes, L.-W. Chang, T.L. Lee*, C.H. Wann*, C.Y. Chang*, H.-S.P. Wong, Stanford University, *TSMC **113**

2:50 p.m.
36.4 Chip-Level and Package-Level Seamless Interconnect Technologies for Advanced Packaging (Invited), S. Yamamichi, K. Mori, K. Kikuchi, H. Murai, D. Ohshima, Y. Nakashima, K. Soejima*, M. Kawano*, T. Murakami, NEC Corporation, *NEC Electronics Corporation **114**

3:15 p.m.
36.5 RF Performance Upgrading of Low-power 40nm-node CMOS Devices by Extremely Low-resistance Partially-thickened Local (PTL)-interconnects, K. Hijioka, J. Kawahara, M. Narihiro, I. Kume, A. Tanabe, H. Nagase, H. Yamamoto, N. Inoue, T. Takeuchi, T. Onodera, S. Saito, N. Furutake, Y. Hayashi, NEC Electronics Corporation **114**

Session 37: Modeling and Simulation – Emerging Devices
Wednesday, December 9, 1:30 p.m.
Key Ballroom 5

1:35 p.m.
37.1 Multilayer Graphene Nanoribbon for 3D Stacking of the Transistor Channel, Y. Ouyang, H. Dai*, J. Guo, University of Florida, *Stanford University **115**

2:00 p.m.
37.2 Physical Insights on Graphene Nanoribbon Mobility Through Atomistic Simulations, A. Betti, G. Fiori, G. Iannaccone, Y. Mao*, Universita di Pisa, *Dana Farber Cancer Institute Pathology **115**

2:25 p.m.
37.3 A Computational Evaluation of the Designs of a Novel Nanoelectromechanical Switch Based on Bilayer Graphene Nanoribbon, K.-T. Lam, G. Liang, National University of Singapore **116**

2:50 p.m.
37.4 Simulation Study of Switching Mechanism in Carbon-Based Resistive Memory with Molecular Dynamics and Extended Hückel Theory-Based NEGF Method, X. Guan, Y. He, L. Zhao, J. Zhang, Y. Wang, H. Qian, Z. Yu, Tsinghua University **116**

3:15 p.m.
37.5 1D Broken-Gap Tunnel Transistor with MOSFET-Like On-Currents and Sub-60mV/dec Subthreshold Swing, S.O. Koswatta*, S.J. Koester, W. Haensch, IBM TJ Watson Research Center, also with University of Notre Dame **117**

3:40 p.m.
37.6 Performance Comparisons of Tunneling Field-Effect Transistors made of InSb, Carbon, and GaSb-InAs Broken Gap Heterostructures, M. Luisier, G. Klimeck, Purdue University **117**

4:05 p.m.
37.7 A Non-iterative Compact Model for Carbon Nanotube FETs Incorporating Source Exhaustion Effects, L. Wei, D.J. Frank*, L. Chang*, H.-S.P. Wong, Stanford University, *IBM TJ Watson Research Center **118**

4:30 p.m.
37.8 Modeling and Optimization of Polymer based Bulk Heterojunction (BH) Solar cell, B. Ray, P.R. Nair, E. Garcia, M.A. Alam, Purdue University **118**

Session 38: Solid-State and Nanoelectronic Devices – Devices and Circuits Based on Nanowires and Solid-Electrolyte Switches
Wednesday, December 9, 1:30 p.m.
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1:35 p.m.
38.1 Nanowire Based Electronics: Challenges and Prospects (Invited), W. Lu, University of Michigan **119**

2:00 p.m.
38.2 CMOS Compatible Ge/Si Core/Shell Nanowire Gate-All-Around pMOSFET Integrated with HfO_2/TaN Gate Stack, J.W. Peng, N. Singh, G.Q. Lo, D.L. Kwong, S.J. Lee*, Institute of Microelectronics, *National University of Singapore **119**

2:25 p.m.
38.3 Excimer Laser-Annealed Dopant Segregated Schottky (ELA-DSS) Si Nanowire Gate-All-Around (GAA) pFET with Near Zero Effective Schottky Barrier Height (SBH), Y.K. Chin, K.L. Pey*, N. Singh, G.Q. Lo, L.H. Tan, G. Zhu*, X. Zhou*, X.C. Wang**, H.Y. Zheng**, Institute of Microelectronics, *Nanyang Technological University, **Singapore Institute of Manufacturing Technology **120**

2:50 p.m.
38.4 Integrated Circuits using Top-Gate ZnO Nanowire Transistors with Ultrathin Organic Gate Dielectric, D. Kalblein, H.J. Bottcher, R.T. Weitz, U. Zschieschang, K. Kern*, H. Klauk, Max Planck Institute for Solid State Research, *also with EPFL **120**

3:15 p.m.
38.5 Highly Scalable Nonvolatile TiOx/TaSiOy Solid-Electrolyte Crossbar Switch Integrated in Local Interconnect for Low Power Reconfigurable Logic, M. Tada, T. Sakamoto, Y. Tsuji, N. Banno, Y. Saito, Y. Yabe, S. Ishida, M. Terai, S. Kotsuji, N. Iguchi, M. Aono*, H. Hada, N. Kasai, NEC Corporation, *MANA **121**

SHORT COURSE

2009 IEDM SHORT COURSE
Low Power / Low Energy Circuits: From Device to System Aspects

Sunday, December 6, 2009
Holiday Ballroom 3, 4, 6
9:00 a.m. – 5:30 p.m.

Course Organizer: Reinout Woltjer, NXP Semiconductors, Eindhoven

Continuous CMOS scaling through a number of decades has opened the way to a huge amount of various applications. Communication, computer, consumer, automotive, industrial, security, medical and many other products benefit from a continuously increasing functionality and data and signal processing capability per chip. On the other hand, this trend has also driven an increasing need to reduce and manage power consumption of related chips – in other words to minimize used energy per functional operation. This of course applies to all mobile and many medical applications where battery lifetime is a crucial criterion for the entire system performance. Moreover, it applies as well to highly integrated logic (and memory) chips with highest data rates and processing speeds where cooling has become an increasingly growing challenge.

In more detail we have to distinguish between various aspects of power consumption such as active power, leakage and standby power. Power consumption on chip level and on system level (on- and off-chip busses, package, parasitics, temperature …) are of different importance in the different application field of related chips. A number of physical limits and boundary conditions exist on the electron device level such as kT/q in standard charge based devices, voltage margins to compensate for variability effects and many more. It is clear that a thorough understanding and optimization on device level must meet circuit, system, and application specific considerations to face this challenge.

Moreover, not only practical and technical aspects require striving for low power, also economic, environmental, and political considerations have begun to play an important role. Electronic tools and devices are known to consume an important and increasing amount of the entire energy produced by the industrial world. Hence, regulations have been or will be introduced and programs are on their way to make electronics “greener” in the context of decreasing power hunger.

This short course reviews the requirements, current status and state-of-the-art approaches, challenges and future options of Low Power and Low Energy Circuits. We approach it from a comprehensive standpoint considering devices and device options, circuit design strategies and related aspects of circuit-device-interaction, packaging and system-level issues, and emerging and disruptive approaches.

We start with a short introduction summarizing basic issues and giving a brief overview about the entire complexity behind the easily said requirement “Low Power / Low Energy”. The first lecture addresses this topic from a device level related view applied to standard logic and mixed-signal processes. Process options from bulk technologies to SOI and SoN and related device approaches are discussed in terms of technical performance but also in terms of processing effort and costs. The second lecture provides a comprehensive discussion of power-aware design strategies and makes the link between technology and design solutions concerning the different power contributions. After that the various memory technologies are highlighted. As these have to fulfill different technical boundary conditions as compared to the logic world also technical answers and challenges are different. In the fourth lecture, the impact of the backend-of-line on power issues is addressed and opportunities in 3D integration as a remarkable amount of power is also used to drive on- and off-chip interconnects. Finally, in the fifths lecture, an overview about emerging and disruptive device concepts is given. Today’s status, their potential, and technical challenges are discussed considering devices such as nanotubes, iMOS and tunnel transistors, Carbon and Graphene devices, and nano relays.

Introduction and Overview
Instructor: Reinout Woltjer, NXP Semiconductors, Eindhoven

Low Power Logic and Mixed-Signal Technologies
Instructor: Thomas Skotnicki, STMicroelectronics

- Introduction
- Historical Review of LP CMOS
- Engineering Mobility
- Electrostatics – Benchmarking Device Structures
- Inverter Delay – LP Specific Case
  - Effective Current
  - Load Capacitance
  - Impact of DIBL
- Benchmarking Bulk Planar, SOI and DG/FinFET
- Variability – Sources, Requirements, Impact
- LP Design Issues and Trends
- Perspective

Less-Power Design
Instructor: Harry Veendrick, NanoCMOS-Training B.V., Heeze

- Necessity of Less-Power Design in all Application Areas
- Battery Topics
- CMOS Power Sources and Trends
- Relation between Less-Power Technology and Design Solutions
- Leakage (Standby) Power Reduction Techniques
- Active (Switching) Power Reduction Techniques

Low Power Approaches for Memories
Instructor: Akihiro Nitayama, Toshiba Corporation

- Introduction
  - Memory System Requirements
  - Memory Positioning and Low Power Approach – Volatile Memories
  - Low Power SRAM
  - Low Power DRAM / FBC / NV-DRAM
- -Nonvolatile Memories
  - FeRAM
  - MRAM
- -Code/ Data Storage Memory
  - PRAM
  - NAND
  - BiCS/ReRAM
- 3D Chip Stacking
- Conclusion

BEOL, SiP, and 3D Integration Technologies
Instructor: James Jian-Qiang Lu, Rensselaer Polytechnic Institute

- Introduction
  - Advances and Challenges in Interconnects and System Integrations
  - 3D Integration Category
- 3D Packaging (SiP, PoP)
  - System-in-Packaging Advances
  - Future Trends
- 3D Integration and Through-Strata-Vias (TSVs)
  - Technology Platforms
  - Key Unit Technologies
  - Advantages and Issues
- 3D Opportunities for Low Power/Low Energy Applications
  - 3D Integration Options
  - Perspectives

Emerging Device Concepts
Instructor: H.S. Philip Wong, Stanford University

- Circuit Requirements: Performance Benchmarking and Requirements, Circuit Level Optimization, CMOS Baseline
- iMOS
- Tunnel FET
- Carbon Nanotube Transistors
- Graphene Transistors
- Nanoelectromechanical (NEM) Relay

SHORT COURSE

Scaling Challenges: Device Architectures, New Materials, and Process Technologies

Sunday, December 6, 9:00 a.m. – 5:30 p.m.
Key Ballrooms 8, 11 and 12

Course Organizer: *Scott Thompson, University of Florida*

Going forward the industry faces unprecedented scaling challenges in device architecture, materials, process modules, and lithography to continuation Moore's law and cost reductions. The best technology direction for sub 32nm technologies nodes is highly uncertain in many areas some of which are high k/metal gate stack materials and process integration flow, planar versus non-planar MOSFET device structures, optical, EUV and double patterning, and in the area of new materials such as SiGe, SiC, low k spacers, and band edge metals. After nearly uniform adoption of unixial strained silicon for 90 to 32nm technology nodes, the industry is seeing more divergence in current 32nm logic IDM and foundry offerings and future plans. To help guide us through this uncertain time, this short course brings the leading technologist from industry and academia to provide insight and likely solutions to address the significant scaling challenges for 22 and 15 nm logic technologies.

The first lecture by IBM Fellow Ghavam Shahidi covers the limits of a bulk or SOI planar MOSFETs and the likely structures to be used for sub 32nm logic technologies. Next, Thomas Hoffmann of IMEC will share his insight into the industry status and future direction for high K dielectrics and metal gates covering both materials and process integration issues. The third talk is by Prof. Ken Uchida is on channel resistance, physics of mobility enhancement techniques and implementations issue for advance nodes. The forth talk is by Applied Material Sr. VP Hans Stork on key process modules for 32nm and beyond technologies node. The final talk is on the hot topic of limits of optical lithography and the status of EUV by Burn Lin of TSMC.

Introduction and Overview

Instructor: Scott E. Thompson, University of Florida

Device Architecture: Ultimate Planar CMOS Limit and Sub 32nm Device Options
Instructor : *Ghavam Shahidi, IBM Corp.*

Challenges/Solutions Planar Bulk and SOI Scaling
Planar Bulk and SOI Limit
MuGFET and future device structures
Insight and future direction

High K / Metal Gates: Industry Status and Future Direction
Instructor: *Thomas Hoffmann, IMEC*

Performance Benefits I or C?
Integration/Material Challenges
Gate last or first integration flow?
HK/MG scaling
Insight and future direction

Channel Resistance: Mobility Enhancement Techniques
Instructor: *Ken Uchida, Tokyo Institute of Technology*

Physics of Strained Si
Process strain for planar device & MuGFET
Implementation issues for advance nodes
SiC and SiGe embedded stressors
Orientation and process strain co-optimization
New material- III-V/Ge
Insight and future direction

Advanced Process Modules: "Key Process Technology for 32nm and Beyond"
Instructor: *Hans Stork, Applied Materials*

Issues/requirements/solutions for chemical mechanical polish
Lithography enhancing films
Profile and high aspect ratio etch
Plasma and ultra shallow Implant technology
SiGe and SiC material issues
Thermal processing millisecond flash and laser annealing
Insight and future direction

Lithography: Limits of Optical Lithography and Status of EUV
Instructor: *Burn Lin, TSMC*

Limits of Optical Lithography
Issues status of Double-Patterning
Requirements for OPC
EUV assessment and status
Layout Design Rules
Insight and future direction

Plenary Session

Monday, December 7, 9:00 a.m.
Key Ballrooms 7 - 12

Welcome and Awards

General Chair: Vivek Subramanian, University of California, Berekeley

Invited Papers

Technical Program Chair: Meikei Ieong, TSMC

1.1 GPU Technology Trends and Future Requirements, John Chen, nVidia

The inherently massive parallelism makes GPU a natural beneficiary of Moore's law. Even with billions of transistors on a latest GPU chip, it is still not good enough for photo realism; and the desire of having more transistors continues. In addition, the use of GPUs for parallel computing is just at the beginning of creating many exciting applications. This talk begins with GPU basics and its evolution with technology, and then connects the GPU requirements such as FLOPS, power and variations to device and process technology. It will also address some of the technological opportunities and challenges for future GPU advancement.

1.2 Printed Organic Transistors: Toward Ambient Electronics, Takao Someya, Tsuyoshi Sekitani, Makoto Takamiya, Takayasu Sakurai, Ute Zschieschang* and Hagen Klauk*, University of Tokyo, *Max Planck Institute for Solid State Research

In the forthcoming ambient electronics era, multiple electronic objects are scattered on walls, ceilings or in imaginative locations and interact each other to enhance safety, security and convenience. For implementation of many electronic objects in our daily life, large-area, flexible devices, which would be printed on plastic sheet, cloth, and/or paper, are expected to play an important role. In this paper, we describe recent progress and future prospects of flexible, large-area electronics based on printed organic transistors.

1.3 **New Perspectives from Micro and Nanotechnologies in Healthcare and Diagnosis,** Jean Chabbal, CEA, LETI, MINATEC

Medical diagnostic plays an increasing role in healthcare systems and provides key information to detect diseases at an early stage and define the best therapy to apply. Medical diagnostic remains mainly centralized within hospitals, large laboratories or imaging centers, which are staffed with highly qualified and trained people. As a result, currently available diagnostic solutions are not suitable for most global healthcare conditions and settings where low cost, ease of use, and field-rugged solutions are imperative. Medical diagnostic shall move from centralized structures toward a decentralized organization able to provide results closed to doctor and patient. Microelectronics and Microsystems provides the solutions for miniaturization, connectivity and portability; 3D heterogeneous integration of detection layers within CMOS electronics is the basis for a new generation of detectors for medical imaging and in vitro diagnostic. The integration of sample preparation remains the key for point of care, multidisciplinary work involving physicist, biologist and chemist is crucial to overcome this bottleneck and a low cost autonomous micro fluidics platform is required.

Session 2: Process Technology - CMOS Junctions: Advanced Anneals and Metrology
Monday, December 7, 1:30 p.m.
Holiday Ballrooms 1, 2 and 3
Co-Chairs: Dan Gealy, Micron Technology Inc.
Michael Hattendorf, Intel

1:30 p.m.
Introduction

1:35 p.m.
2.1 Silicide Yield Improvement with NiPtSi Formation by Laser Anneal for Advanced Low Power Platform CMOS Technology, C. Ortolland, E. Rosseel, N. Horiguchi, C. Kerner, S. Mertens, J. Kittl, E. Verleysen*, H. Bender, W. Vandervost*, A. Lauwers, P.P. Absil, S. Biesemans, S. Muthukrishnan*, S. Srinivasan*, A.J. Mayur*, R. Schreutelkamp*, T. Hoffmann, IMEC, K.U. Leuven, **Applied Materials

A novel silicide formation technique using milli-second anneal is reported for the first time, delivering superior silicide film morphology that translates electrically into significant yield improvement over a conventional soak anneal, without any degradation of transistor performances. In addition, we demonstrate how this new technique enables the integration of thin silicides required for further junction scaling, and demonstrate up to 6nm gate length reduction and more than 1 decade junction leakage reduction.

2:00 p.m.
2.2 A Study on Millisecond Annealing (MSA) Induced Layout Dependence for Flash Lamp Annealing (FLA) and Laser Spike Annealing (LSA) in Multiple MSA Scheme with 45nm High-Performance Technology, T. Miyashita, T. Kubo, Y.S. Kim, M. Nishikawa, Y. Tamura, J. Mitani, M. Okuno, T. Tanaka, H. Suzuki, T. Sakata, T. Kodama, T. Itakura, N. Idani, T. Mori, Y. Sambonsugi, A. Shimizu, H. Kurata, T. Futatsugi, Fujitsu Microelectronics Limited

Layout dependent temperature uniformity of millisecond annealing and its impact on device characteristics and SRAM yields have been investigated with 45 nm high performance technology without the use of absorbers. By comparing flash lamp annealing (FLA) and laser spike annealing (LSA), LSA is promising due to its lower pattern sensitivity and high potential for performance enhancement. Hot spot generation was newly found for LSA, but it can be avoided with active area size restriction.

2:25 p.m.

2.3 3D 65nm CMOS with 320°C Microwave Dopant Activation, Y.-J. Lee, Y.-L. Lu*, F.-K. Hsueh, K.-C. Huang*, C.-C. Wan*, T.-Y. Cheng*, M.-H. Han*, J.M. Kowalski**, J.E. Kowalski**, D. Heh, H.-T. Chuang, Y. Li*, T.-S. Chao*, C.-Y. Wu^, F.-L. Yang, National Nano Device Laboratories, *National Chiao Tung University, **DSG Technologies, Inc., ^Dayeh University

For the first time, CMOS TFTs of 65nm have been demonstrated by using a novel microwave dopant activation technique. We have successfully activated the poly-Si gate electrode and source/drain junctions at a low temperature of 320°C for only 100 seconds, which is promising for integrating high performance upper layer nanoscaled transistors as required by low temperature 3D-ICs fabrication.

2:50 p.m.

2.4 Insight into the S/D Engineering by High-resolution Imaging and Precise Probing of 2D-Carrier Profiles with Scanning Spreading Resistance Microscopy, L. Zhang, M. Saitoh, A. Kinoshita, N. Yasutake, A. Hokazono, N. Aoki, N. Kusunoki, I. Mizushima, M. Koike, S. Takeno, J. Koga, Toshiba Corporation

High-resolution imaging and precise resistance probing of S/D carrier profiles by SSRM are carried out on (110)/(100) CMOSFETs revealing 2D I/I channering effects and As out-diffusion during silicidation on (110). Diffusion suprresion by Si:C doping are also directly confirmed agrees well with Vth-roll-off; SSRM resistance shows correlation with parasitic resistance. Sample making has breakthrough for narrow devices down to 0.5 um width.

3:15 p.m.
2.5 Strain Metrology of Devices by Dark-Field Electron Holography: A New Technique for Mapping 2D Strain Distributions (Invited), M. Hÿtch, F. Hüe*, F. Houdellier, E. Snoeck, A. Claverie, CEMES-CNRS, *and also with University of Cambridge

We present the latest results from the new technique of dark-field electron holography (HoloDark) which is capable of measuring strain to high precision, with nanometre spatial resolution and for micron fields of view. Strain measurements in active regions of strained-silicon MOSFET devices will be confirmed by finite element modeling.

Session 3: CMOS Devices and Technology – Device Scaling and Variability

Monday, December 7, 1:30 p.m.
Holiday Ballrooms 4 and 5
Co-Chairs: *Youichi Momiyama, Fujitsu Microelectronics*
Mariko Takayanagi, Toshiba Corporation

1:30 p.m.
Introduction

1:35 p.m.
3.1 Dual Metallic Source and Drain Integration on Planar Single and Double Gate SOI CMOS Down to 20nm: Performance and Scalability Assessment, L. Hutin, M. Vinet, T. Poiroux, C. Le Royer, B. Previtali, C. Vizioz, D. Lafond, Y. Morand*, M. Rivoire*, F. Nemouchi, V. Carron, T. Billon, S. Deleonibus, O. Faynot, CEA/LETI, MINATEC, *STMicroelectronics

We hereby report the fabrication, electrical characterization and TCAD simulation of planar Single and Double Gate n- and p-MOSFETs with metallic Dopant Segregated Source and Drain (DSS) on SOI, with gate lengths down to 20nm. A wide range of experimental data for various architectures, metallizations and doping conditions is analyzed.

2:00 p.m.

3.2 Extremely Thin SOI (ETSOI) CMOS with Record Low Variability for Low Power System-on-Chip Applications, K. Cheng, A. Khakifirooz, P. Kulkarni, S. Ponoth, J. Kuss, D. Shahrjerdi*, L.F. Edge, A. Kimball, S. Kanakasabapathy, K. Xiu**, S. Schmitz, A. Reznicek, T. Adam, H. He, N. Loubet***, S. Holmes, S. Mehta, D. Yang**, A. Upham, S.-C. Seo, J.L. Herman, R. Johnson, Y. Zhu*, P. Jamison, B.S. Haran, Z. Zhu**, L.H. Vanamurth, S. Fan, D. Horak, H. Bu, P.J. Oldiges**, D.K. Sadana*, P. Kozlowski, D. McHerron, J. O'Neill, B. Doris, IBM, *IBM TJ Watson Research Center, **IBM SRDC, ***STMicroelectronics

We present a novel ETSOI CMOS integration scheme with following features: (1) faceted Si:C RSD for NFET and faceted SiGe RSD for PFET, and (2) enhanced stress liner effect coupling with faceted RSD. Devices with those strain techniques shows remarkable performance and the smallest device variation.

2:25 p.m.

3.3 Carrier Profile Designing to Suppress Systematic V_{th} Variation Related with Device Layout by Controling STI-enhanced Dopant Diffusions Correlated with Point Defects, H. Fukutome, Y. Momiyama, A. Satoh, Y. Tamura, H. Minakata, K. Okabe, E. Mutoh, K. Suzuki, A. Usujima, H. Arimoto, S. Satoh, Fujitsu Microelectronics

We directly measured that anisotropic dopant diffusion into the shallow trench isolation sink predominantly caused dependence of threshold voltage (Vth) on the active width along channel direction (LOD) for the nMOSFETs and excess point defects in the S/D enhancing random extension edge roughness increased Vth fluctuation in the narrow-LOD nMOSFET.

2:50 p.m.
3.4 Physical Model of the Impact of Metal Grain Work Function Variability on Emerging Dual Metal Gate MOSFETs and its Implication for SRAM Reliability, X. Zhang, J. Li*, M. Grubbs, M. Deal, B. Magyari-Kope, B. Clemens, Y. Nishi, Stanford University, *IBM

A new model of work function variability (WFV) based on grain orientation differences of the metal gate is reported. Our model predicts that at the 22nm technology node, WFV will become the dominating variability factor. The SRAM write/read failures are underestimated by 9 orders of magnitude by the previous model.

3:15 p.m.
3.5 Experimental Investigation and Design Optimization Guidelines of Characteristic Variability in Silicon Nanowire CMOS Technology, J. Zhuge*, R. Wang*, R. Huang*, J. Zou*, X. Huang*, D.-W. Kim**, D. Park**, X. Zhang*, Y. Wang*, *Peking University and Ministry of Education, **Samsung Electronics Co.

Characteristic variability in the gate-all-around (GAA) Silicon Nanowire MOSFETs (SNWTs) is experimentally studied. Variation sources in SNWTs are extracted for the first time. The influence of the SNWT variation sources on SRAM performance is estimated and compared with planar devices. Design optimization guidelines are given based on the SRAM variation analyzed results.

Session 4: Modeling and Simulation - Memory and Transport Modeling

Monday, December 7, 1:30 p.m.
Holiday Ballroom 6
Co-Chairs: Ganesh Samudra, National University of Singapore
Tatsuya Kunikiyo, Renesas Technology Corp.

1:30 p.m.
Introduction

1:35 p.m.
4.1 Quantum Simulations of Hole Transport in Si, Ge, SiGe and GaAs Double-Gate pMOSFETs: Orientation and Strain Effects, N. Cavassilas, S. d'Ambrosio, M. Bescond, IM2NP

The influence of channel material, crystallographic orientation and strain on the double-gate pMOSFET performances is investigated. We have developed a self-consistent code which couples the six-band k.p Hamiltonian to the Green function formalism. The results present a clear transport phenomena description and point out the configurations providing significant electrical improvement.

2:00 p.m.
4.2 Experimental and Physics Based Modeling Assessment of Strain Induced Mobility Enhancement in FinFETs, N. Serra, F. Conzatti, D. Esseni, M. De Michielis, P. Palestri, L. Selmi, S. Thomas*, T.E. Whall*, E.H.C. Parker*, D.R. Leadley*, L. Witters**, A. Hikavyy**, M.J. Hÿtch^, F. Houdellier^, E. Snoeck^, T.J. Wang^^, W.C. Lee^^, G. Vellianitis[#], M.J.H. van Dal[#], B. Duriez[#], G. Doornbos[#], R.J.P. Lander[#], DIEGM, *University of Warwick, **IMEC, ^CEMES-CNRS, ^^TSMC, [#]NXP-TSMC

This study combines direct strain and mobility measurements, and a rigorous modeling approach to provide insight and guidelines for device optimization. Mobilities in n- and p-FinFETs, measured at different temperatures, are compared with a state-of-art transport modeling which strain is introduced by modification of the band-structure.

2:25 p.m.
4.3 Universal Mobility Modeling and its Application to Interface Engineering for Highly Scaled MOSFETs Based on First-Principles Calculation, T. Ishihara, D. Matsushita, K. Kato, Toshiba Corporation

We propose the interface engineering method to improve the mobility degradation due to the interface states based on universal mobility modeling, and have confirmed that the proposed method efficiently suppress the mobility degradation due to the interface states by the experiment.

2:50 p.m.
4.4 Self-Consistent Monte Carlo Device Simulations Under Nano-Scale Device Structures: Role of Coulomb Interaction, Degeneracy, and Boundary Condition, K. Nakanishi, T. Uechi, N. Sano, University of Tsukuba

The self-consistent 3D MC device simulations including the full Coulomb interaction are carried out. We demonstrate that the boundary condition for the electron distribution function plays an essential role to obtain correct transport characteristics and that the Coulomb interaction is indeed a key ingredient for reliable predictions of device properties.

3:15 p.m.
4.5 New Insight on the Charge Trapping Mechanisms of SiN-Based Memory by Atomistic Simulations and Electrical Modeling, E. Vianello, L. Perniola, P. Blaise, G. Molas, J.P. Colonna, F. Driussi*, P. Palestri*, D. Esseni*, L. Selmi*, N. Rochat, C. Licitra, D. Lafond, R. Kies, G. Reimbold, B. De Salvo, F. Boulanger, CEA-LETI MINATEC, *DIEGM

We investigated the trapping properties of two SiN films by means of atomistic simulations (Density Functional Theory (DFT) and GW). We show that different defects are responsible for the memory behavior depending on the Si-to-N ratio. A simple physical model for the traps is derived; its implementation in a device numerical simulator allows us to reproduce the experimental program-retention transients of memory cells with diverse SiN composition.

Session 5: Memory Technology – PRAM and RRAM

Monday, December 7, 1:30 p.m.
Key Ballrooms 7, 9 and 10
Co-Chairs: *Chenhsin Lien, National Tsing Hua University*
Hyunsang Hwang, Gwangju Institute of Science and Technology

1:30 p.m.
Introduction

1:35 p.m.
5.1 Chalcogenide PCM: A Memory Technology for Next Decade (Invited), R. Bez, Numonyx

As the end of this decade is approaching it can be noted that only one of the proposed alternative NVM technologies is demonstrating the capability to enter in the broad market and to be a mainstream one for the next decade: the Phase Change Memory (PCM) technology. PCM provides a new set of features interesting for novel applications, combining components of NVM and DRAM and being at the same time a sustaining and a disruptive technology. In this invited paper the PCM technology status will be reviewed and future development lines will be drawn.

2:00 p.m.
5.2 1D Thickness Scaling Study of Phase Change Material ($Ge_2Sb_2Te_5$) Using a Pseudo 3-Terminal Device, B.-J. Bae, S. Kim*, Y. Zhang*, Y.K. Kim, I.-G. Baek, S. Park, I.-S. Yeo, S. Choi, J.-T. Moon, H.-S.P. Wong*, K. Kim, Samsung Electronics Co. Ltd., *Stanford University

1D thickness scaling study on a-GST has been successfully demonstrated without the help of ultra-fine lithography. Vth linearly scales down to ~0.65 V at 6 nm scale, showing that stable read operation is possible at elevated temperature (70°). Reset R drift shows no dependency on the a-GST thickness up to 6nm regime. Thin a-GST shows enhanced thermal stability compared to thick a-GST.

2:25 p.m.
5.3 Phase Change Memory Technology for Embedded Non Volatile Memory Applications for 90nm and Beyond, R. Annunziata, P. Zuliani, M. Borghi, G. De Sandre, L. Scotti, C. Prelini, M. Tosi*, I. Tortorelli*, F. Pellizzer*, STMicroelectronics, *Numonyx

In this work a 90nm PCM technology for embedded non-volatile memory applications is presented. A 1T/1R MOS-selected PCM cell has been chosen as the best solution in terms of additional masks count and process simplicity. The full integration of a 4Mb ePCM macrocell on the advanced 90nm CMOS platform has been successfully achieved with solid results in terms of functionality, stability and reliability.

2:50 p.m.

5.4 Effect of Oxygen Migration and Interface Engineering on Resistance Switching Behavior of Reactive Metal/Polycrystalline $Pr_{0.7}Ca_{0.3}MnO_3$ Device for Nonvolatile Memory Applications, D.-J. Seong, J. Park, N. Lee, M. Hasan, S. Jung, H. Choi, J. Lee, M. Jo, W. Lee, S. Park, S. Kim, Y.H. Jang, Y. Lee*, M. Sung*, D. Kil*, Y. Hwang*, S. Chung*, S. Hong*, J. Roh*, H. Hwang, Gwangju Institute of Science and Technology, *Hynix Semiconductor Inc.

Using redox reaction, we can control the interface of metal/polycrystalline-perovskite oxide, which in turn causes reproducible resistive switching characteristics. A redox reaction can be controlled by applied bipolar bias which control electro-migration of oxygen ions. We obtained excellent memory characteristics with polycrystalline oxide by controlling reactivity of metal electrode.

3:15 p.m.

5.5 Highly Scalable Hafnium Oxide Memory with Improvements of Resistive Distribution and Read Disturb Immunity, Y.S. Chen*, H.Y. Lee*, P.S. Chen**, P.Y. Gu*, C.W. Chen*, W.P. Lin*, W.H. Liu*, Y.Y. Hsu*, S.S. Sheu*, P.C. Chiang*, W.S. Chen*, F.T. Chen*, C.H. Lien, M.-J. Tsai*, National Tsing Hua University, *Industrial Technology Research Institute, **MingShin University of Science and Technology

The $30x30nm^2$ HfO_x RRAM with excellent memory performances is demonstrated for the scaling feasibility. All devices in the 1Kb array can exceed 1M cycles by pulse width of 40ns. A verification method of HRS and LRS are proposed for the array to ensure good operation window. A thin AlO_x buffer layer can enhance the read disturb immunity.

3:40 p.m.
5.6 High Density and Ultra Small Cell Size of Contact ReRAM (CR-RAM) in 90nm CMOS Logic Technology and Circuits, Y.H. Tseng, C.-E. Huang, C.-H. Kuo*, Y.-D. Chih*, C.J. Lin, National Tsing-Hua University, *TSMC

A new Contact ReRAM cell is demonstrated with 90nm CMOS logic technology. The new contact ReRAM cell exhibits highly stable read window and very small cell size of 0.19μm^2. Excellent endurance and retention characteristics support the new Contact ReRAM (CR-RAM) cell will be a superior NVM technology for the future.

4:05 p.m.
5.7 A 45nm Generation Phase Change Memory Technology, G. Servalli, Numonyx

In this paper we present for the first time a 45nm generation PCM technology with an effective cell as small as 0.015μm^2 developed on a 1Gb product. Device architecture, fabrication technologies, electrical cell characterization and reliability results are reported.

Session 6: Characterization, Reliability, and Yield – Hi-K

Monday, December 7, 1:30 p.m.
Key Ballrooms 8, 11 and 12
Co-Chairs: Sangwoo Pae, Intel Corporation
Min Cao, TSMC
1:30 p.m.
Introduction

1:35 p.m.
6.1 Fermi Level Pinning in Si, Ge and GaAs Systems - MIGS or Defects? (Invited), J. Robertson, L. Lin, Cambridge University

Interfaces in Si, Ge or GaAs FETs can behave undesirably, with Fermi level pinning. Pinning can be intrinsic (MIGS) or extrinsic (defects, dangling bonds). Identifying the mechanism can be difficult, as both follow similar chemical trends. It is important to be correct, as only extrinsic mechanisms are correctable by processing.

2:00 p.m.
6.2 Negatively Charged Deep Level Defects Generated by Yttrium and Lanthanum Incorporation into HfO_2 for V_{th} Adjustment, and the Impact on TDDB, PBTI and 1/*f* Noise, M. Sato, S. Kamiyama, Y. Sugita, T. Matsuki, T. Morooka, T. Suzuki, K. Shiraishi*, K. Yamabe*, K. Ohmori**, K. Yamada**, J. Yugami, K. Ikeda, Y. Ohji, Selete, *University of Tsukuba, **Waseda University

We found that Y and La incorporation into HfO_2 introduces negatively charged deep level interstitial oxygen defects, which lead smaller Weibull b values and early failure in TDDB, with negative shift in PBTI. On the other hand, they are effective in noise reduction, as an effect of Nit reduction.

2:25 p.m.

6.3 Impact of Dipole-Induced Dielectric Relaxation on High-frequency Performance in La-Incorporated HfSiON/Metal Gate nMOSFET, G.B. Choi, H.C. Sagong, K.T. Lee, M.S. Park, H.S. Choi, S.H. Song, R.H. Baek, C.H. Park, S.H. Lee, J.S. Lee, C.Y. Kang*, H-H. Tseng*, R. Jammy*, Y.H. Jeong, Pohang University of Science and Technology, *SEMATECH, NCNT

The relationship of high frequency and dielectric relaxation of dipole formed at the high-k/SiO_2 interface was systematically investigated in La-doped HfSiON devices. Due to the dipole-induced DR, it was found that high frequency performance, especially voltage gain severely degrades caused by substantial degradation in gate capacitance, transconductance, and output resistance in a frequency range below 1 GHz.

2:50 p.m.

6.4 Reversible and Irreversible Degradation Attributing to Oxygen Vacancy in HfSiON Gate Films During Electrical Stress Application, R. Hasunuma, C. Tamura, T. Nomura, Y. Kikuchi, K. Ohmori*, M. Sato**, A. Uedono, T. Chikyow^, K. Shiraishi, K. Yamada**, K. Yamabe, University of Tsukuba, *Waseda University, **SELETE, ^NIMS

Dielectric degradation under electrical stress application involves reversible and irreversible phenomena before breakdown. The irreversible phenomenon was attributed to mass transport in HfSiON films inducing structural transformation. The degradation was found to occur under high electrical field. This warns against the conventional TDDB test with excessive stress voltage.

3:15 p.m.

6.5 Observation of Switching Behaviors in Post-Breakdown Conduction in NiSi-gated Stacks, W.H. Liu, K.L. Pey, X. Li, M. Bosman*, Nanyang Technological University, *Institute of Microelectronics

Switching from high to low conduction state was found in gate oxide breakdown NiSi-gated MOSFETs. The percolation path is “switched off” by repassivaitng of dangling bonds in the breakdown path by oxygen species. This new finding can be incorporated into circuits design and program to repair transistor during field use.

3:40 p.m.

6.6 A Discharge-Based Multi-Pulse Technique (DMP) for Probing Electron Trap Energy Distribution in High-*k* Materials for Flash Memory Application, X.F. Zheng, W.D. Zhang, B. Govoreanu*, J.F. Zhang, J. van Houdt*, Liverpool John Moores University, *IMEC

A new discharge-based multi-pulse technique has been developed, which, for the first time, gives the electron trap energy distribution in the bulk of high-*k* materials. Trap distributions in HfO_2, Al_2O_3 and HfAlO have been extracted and compared to identify the effects of material variation on the distribution.

Session 7: Quantum, Power, and Compound Semiconductors – Power Devices: Si, SiC, GaN

Monday, December 7, 1:30 p.m.
Key Ballrooms 3, 4 and 6
Co-Chairs: Enrico Zanoni, University of Padova
Toshihide Kikkawa, Fujitsu Laboratories Ltd.

1:30 p.m.
Introduction

1:35 p.m.
7.1 NexFET A New Power Device, S. Xu, J. Korec, D. Jauregui, C. Kocon, S. Malloy, H. Lin, G. Daum, S. Perellia, K. Barry, C. Pearce, O. Lopez, J. Herbsommer, Texas Instruments

A new generation of Power MOSFET technology has been introduced. The devices are manufactured in a standard 0.35µm CMOS production line with only few process modules being adapted for the requirements of vertical power transistors with an 2x improvement of FOM, enabling the operate at double the frequency. This improvement results mainly from the reduction of the Miller capacitance.

2:00 p.m.
7.2 Power MOSFETs, IGBTs, and Thyristors in SiC: Optimization, Experimental Results, and Theoretical Performance (Invited), J.A. Cooper, T. Tamaki*, G.G. Walden, S. Sue, S.R. Wang, X. Wang, Purdue University, *Renesas Tech. Corp

SiC power devices have reached a level of performance far beyond silicon, and SiC materials are approaching the point where commercial production is feasible. This paper presents experimental results on SiC MOSFETs, IGBTs, and thyristors, and gives a methodology for evaluating different devices as a function of blocking voltage and switching frequency.

2:25 p.m.
7.3 Normally-off GaN FET with High Threshold Voltage Uniformity Using A Novel Piezo Neutralization Technique, K. Ota, K. Endo, Y. Okamoto, Y. Ando, H. Miyamoto, H. Shimawaki, NEC Corporation

We have developed a GaN FET with a novel piezo neutralization technique which realizes the uniform V_{th} even for the recessed gate FETs. The developed normally-off devices exhibited an excellent standard deviation of the Vth of 18mV together with a state-of-the-art combination of the $R_{on}A$ of 700mΩmm^2 and the VB over 1000V.

2:50 p.m.
7.4 Low Leakage High Breakdown E-Mode GaN DHFET on Si by Selective Removal of In-Situ Grown Si_3N_4, J. Derluyn, M. Van Hove, D. Visalli, A. Lorenz, D. Marcon, P. Srivastava, K. Geens, B. Sijmus, J. Viaene, X. Kang, J. Das, F. Medjdoub, K. Cheng, S. Degroote, M. Leys, G. Borghs, M. Germain, IMEC

This abstract describes dispersion-free e-mode SiN/$Al_{45}Ga_{55}N$/GaN/$Al_{18}Ga_{82}N$ DHFETs on 4” Si substrates with a narrow Vt distribution of +475mV ± 15mV. The on/off ratio is 1e7. The off-state breakdown is 710V for an R_{on} of 2mΩ.cm^2. At 560V, the drain leakage current is 5µA/mm, significantly reducing the off-state power dissipation.

3:15 p.m.
7.5 Normally-off 5A/1100V GaN-on-Silicon Device for High Voltage Applications, K.S. Boutros, S. Burnham, D. Wong, K. Shinohara, B. Hughes, D. Zehnder, C. McGuire, HRL Laboratories

We report the DC and switching performance of a normally-off 5A/1100V GaN-on-Si device. The device had a breakdown field of 95V/μm and a $V_B^2/R_{on,sp}$ of 272MW/cm^2. A 360V/180W boost converter was operated at 200KHz, with an efficiency >92%. Respectively, these values are the highest for a normally-off GaN-on-Si device.

3:40 p.m.
7.6 GaN Monolithic Inverter IC Using Normally-off Gate Injection Transistors with Planar Isolation on Si Substrate, Y. Uemoto, T. Morita, A. Ikoshi, H. Umeda, H. Matsuo, J. Shimizu, M. Hikita, M. Yanagihara, T. Ueda, T. Tanaka, D. Ueda, Panasonic Corporation

We present GaN-based monolithic IC for motor drive for the first time. Planaer and temperature-stabe isolation is enabled by Fe ion implantation, which results in sucessful integration of the GaN-based lateral transistor.The fabricated monolithic inverter IC exhibits 93% efficiency even at 20% output-power condition, which cannot be achieved by conventional Si-IGBT-based one.

4:05 p.m.

7.7 Correlation Between DC and rf Degradation Due to Deep Levels in AlGaN/GaN HEMTs, A. Chini*, F. Fantini*, V. Di Lecce*, M. Esposto*, A. Stocco, N. Ronchi, F. Zanon, G. Meneghesso, E. Zanoni, University of Padova, *University of Modena and Reggio Emilia

We investigate the role of the 0.5 eV traps in determining GaN HEMT degradation by means of 2D numerical simulation and rf testing. We demonstrate that generation of 0.5 eV deep levels is responsible for the degradation observed during rf aging; we show that the occurrence of trap-induced degradation depends on rf driving conditions. We also show that degradation can be explained by the generation of a damaged region within the AlGaN layer at the gate-drain edge.

4:30 p.m.

7.8 InAlN/GaN Heterostructures for Microwave Power and Beyond (Invited), E. Kohn, M. Alomari, A. Denisenko, M. Dipalo, D. Maier, F. Medjdoub, C. Pietzka, S. Delage[1], M.-A. di Forte-Poisson[1], E. Morvan[1], N. Sarazin[1], J.-C. Jacquet[1], C. Dua[1], J.-F. Carlin[2], N. Grandjean[2], M. Py[2], M. Gonschorek[2], J. Kuzmik[3], D. Pogany[3], G. Pozzovivo[3], C. Ostermaier[3], L. Toth[4], B. Pecz[4], J.-C. De Jaeger[5], C. Gaquiere[5], K. Cico[6], K. Fröhlich[6], A. Georgakilas[7], E. Iliopoulos[7], G. Konstantinidis[7], C. Giessen[8], M. Heuken[8], B. Schineller[8], Ulm University, [1]Alcatel, [2]EPFL, [3]Technological University of Wien, [4]MFA, [5]IEMN, [6]IEE, [7]FORTH, [8]Aixtron

The high chemical stability of the InAlN/GaN heterostructure promise exceptional power handling capabilities, robustness and operation under harsh environmental conditions. All three topics are addressed as especially, high temperature operation of HEMTs, native oxide power MOSHEMTs and nitride/diamond hybrid device structures for thermal management and sensing in highly corrosive media.

Session 8: Displays, Sensors, and MEMS – TFT Technologies

Monday, December 7, 1:30 p.m.
Key Ballroom 5
Co-Chairs: Torii Kazuyoshi, Hitachi
Francois Roy, STMicroelectronics

1:30 p.m.
Introduction

1:35 p.m.
8.1 Integrated High Performance (100) and (110) Oriented Single-Grain Si TFTs without Seed Substrate, T. Chen, R. Ishihara, J. van der Cingel, B. Alessandro, M.R. Tajari Mofrad, H. Schellevis, K. Beenakker, Delft University of Technology

High performance single-grain TFTs have been fabricated inside an orientation- and location-controlled Si grain with 600°C process. Electron and hole mobilities are 998cm^2/Vs and 292cm^2/Vs for (100) and 811cm^2/Vs and 429cm^2/Vs for (110), respectively. Surface and in-plane orientation control improved the uniformity approaching the SOI counterpart.

2:00 p.m.
8.2 A Novel Five-Photo-Mask Low-Temperature Polycrystalline-Silicon CMOS Structure, S.-J. Lee, S.-W. Lee, K.-M. Oh, K.-E. Lee, M.-S.Yang, Y.-K. Hwang, LG Display

A novel five-mask LTPS CMOS structure was proposed and verified by manufacturing test panels. By using the diffractive exposure method, we eliminated storage photo step. Gate mask was removed by separate patterning of P-type and N-type gate metal with each of the conventional doping masks. For the final mask #5 step, via hole and indium-tin-oxide (ITO) photomask steps were eliminated at once, where diffraction photo and selective etch sequence was applied onto sequentially sputtered ITO and Mo/AlNd source/drain (S/D) layers.

2:25 p.m.
8.3 Integration of Single Crystal Si TFTs and Circuits on a Large Glass Substrate, Y. Takafuji, Y. Fukushima, K. Tomiyasu, M. Takei, Y. Ogawa, K. Tada, S. Matsumoto, H. Kobayashi, Y. Watanabe, E. Kobayashi, S.R. Droes*, A.T. Voutsas*, J. Hartzell*, Sharp Corporation, *Sharp Laboratories of America Inc.

Submicron single crystal-Si TFTs are integrated on a 320x400mm glass substrate for the first time, by transferring devices using hydrogen exfoliation and direct bonding without adhesive. Characteristics of the NMOS-TFT is comparable with that of SOI. Shift register is functioning at 400MHz with power supply of 3V.

2:50 p.m.
8.4 High Performance Amorphous Oxide Thin Film Transistors with Self-Aligned Top-Gate Structure, J.C. Park, S.W. Kim, S.I. Kim, H. Yin, J.H. Hur, S.H. Jeon, S.H. Park, I.H. Song, Y.S. Park, U.I. Chung, M.K. Ryu, S. Lee*, S. Kim*, Y. Jeon*, D.M. Kim*, D.H. Kim* , K.-W. Kwan**, C.J. Kim, Samsung Advanced Institute of Technology, *Kookmin University, **Sungkyunkwan University

We have demonstrated self-aligned top-gate amorphous oxide transistors for large size and high resolution displays. The processes such as source/drain and channel engineering have been developed to realize the self-aligned top gate structure. Ar plasma is exposed on the source/drain region of active layer to minimize the source/drain series resistances. To prevent the conductive channel, N_2O plasma is also treated on the channel region of active layer. Surprisingly, a-IZO TFTs fabricated on glass substrate exhibit excellent electrical properties such as a field effect mobility of 115 cm^2/Vs, a threshold voltage of 0.2 V, and low threshold voltage shift less than 1 V under bias temperature stress for 3 hr.

3:15 p.m.
8.5 ZnO Thin Film Transistors and Circuits on Glass and Polyimide by Low-Temperature PEALD, D.A. Mourey, D.A. Zhao, T.N. Jackson, Pennsylvania State University

We report using a novel weak oxidant plasma-enhanced atomic layer deposition (PEALD) process to fabricate stable high mobility ZnO thin film transistors (TFTs) and self-aligned-gate circuits on glass with propagation delay <10 ns/stage, as well as the fastest reported oxide-semiconductor circuits on polyimide substrates at 200C (60 ns/stage).

3:40 p.m.
8.6 High Performance Low Voltage Amorphous Oxide TFT Enhancement/Depletion Inverter Through Uni-/Bi-Layer Channel Hybrid Integration, H. Yin, S. Kim, J. Park, I. Song, S.-W. Kim, J. Hur, S. Park, S. Jeon, C.J. Kim, Samsung Electronics

A novel amorphous oxide TFT E/D inverter through uni-/bi-layer hybrid integration with conventional process is demonstrated. Comparing to the reported high speed bootstrapped inverter, the output swing, voltage gain and noise margin of E/D inverter are greatly improved while the speed of ring oscillator shows slight degradation with a smaller supply voltage of 5V.

4:05 p.m.

8.7 Novel, 100 V, Trench Super Junction High Voltage TFTs using Low Temperature Poly Crystalline Silicon, M.H. Dhyani, D. Green, M. Sweet, E.M. Sankara Narayanan, S.C. Deane*, N.D. Young*, Sheffield University, *Philips Research Laboratories

First results of 100 V, novel Trench Super Junction HVTFTs fully compatible to the LTPS technology are presented. They exhibit ON/OFF current ratio of more than 10^7 with sub-threshold swing of 0.75V/decade and specific resistance (Rsp) of 40Ωmm^2. The influence of geometric parameters on both unipolar and bipolar devices is analysed.

4:30 p.m.

8.8 A Novel LTPS-TFT-Based Charge-Trapping Memory Device with Field-Enhanced Nanowire Structure, T.-C. Liao, S.-K. Chen, M.H. Yu, C.-Y. Wu, T.-K. Kang*, F.-T. Chien*, Y.-T. Liu, C.-M. Lin*, H.-C. Cheng, National Chiao Tung University, *Feng Chia University

A novel gate-all-around LTPS-TFT SONOS memory with field-enhanced nanowire structure was demonstrated using a simple process sequence. Each nanowire inherently had three sharp corners fabricated simply by sidewall spacer formation to obtain high local electric fields and thus much improve P/E efficiency, as analyzed with simulation. Therefore, such device is very promising for system-on-panel applications.

Session 9: Solid-State and Nanoelectronics Devices – Spin Devices and Nano-Electromechanical Devices

Monday, December 7, 1:30 p.m.
Key Ballrooms 1 and 2
Co-Chairs: Atsuhiro Kinoshita, Toshiba Corp.
Kerem Akarvardar, Stanford University

1:30 p.m.
Introduction

1:35 p.m.
9.1 Silicon Spintronics: Spin Injection, Manipulation and Electrical Detection (Invited), B.T. Jonker, O.M.J. van 't Erve, G. Kioseoglou, A.T. Hanbicki, C.H. Li, M. Holub, C. Awo-Affouda, P.E. Thompson, Naval Research Laboratory

The electronics industry to date has relied upon the control of charge flow, and used size scaling to continuously increase the performance of existing electronics. However, size scaling cannot continue indefinitely, and new approaches must be developed. Basic research efforts have shown that spin angular momentum, another fundamental property of the electron, can be used to store and process information in solid state devices. The *International Technology Roadmap for Semiconductors* has identified the electron's spin as a new state variable which should be explored for use beyond CMOS.

2:00 p.m.
9.2 Read/Write Operation of Spin-Based MOSFET Using Highly Spin-Polarized Ferromagnet/MgO Tunnel Barrier for Reconfigurable Logic Devices, T. Marukame, T. Inokuchi, M. Ishikawa, H. Sugiyama, Y. Saito, Toshiba Corporation

Si-based spintronic devices have attracted much attention as promising candidates of beyond CMOS device. We developed spin-based MOSFET for reconfigurable logic such as FPGA with nonvolatility. Using highly spin-polarized ferromagnet/MgO tunnel barrier, we observed spin transport through Si. Read/write operation of spin-based MOSFET using spin-transfer torque switching was first demonstrated.

2:25 p.m.

9.3 A Disturbance-Free Read Scheme and a Compact Stochastic-Spin-Dynamics-Based MTJ Circuit Model for Gb-scale SPRAM, K. Ono, T. Kawahara, R. Takemura, K. Miura, H. Yamamoto, M. Yamanouchi, J. Hayakawa, K. Ito, H. Takahashi, S. Ikeda, H. Hasegawa, H. Matsuoka, H. Ohno*, Hitachi Ltd., *Tohoku University

A compact stochastic-spin-dynamics-based MTJ circuit model was developed. Switching behaviors simulated by this model were verified by experimental measurements. Moreover, a disturbance-free read scheme for Gb-scale SPRAM was also developed. The feasibility of this scheme was confirmed by circuit simulation using the model and on-chip measurement of switching probability.

2:50 p.m.

9.4 4-Terminal Relay Technology for Complementary Logic, R. Nathanael, V. Pott, H. Kam, J. Jeon, T.-J. King Liu, University of California, Berkeley

A new 4-terminal relay technology is presented. By appropriate biasing of the 4th (body) terminal, low-voltage switching (<2V) and low switching delay (100ns) can be achieved. Endurance exceeds $>10^9$ on/off cycles, so that this relay technology appears promising for implementation of energy-efficient complementary logic circuits.

3:15 p.m.

9.5 3-Terminal Nanoelectromechanical Switching Device in Insulating Liquid Media for Low Voltage Operation and Reliability Improvement, J.-O. Lee, M.-W. Kim, S.-D. Ko, H.-O. Kang*, W.-H. Bae*, M.-H. Kang*, K.-N. Kim*, D.-E. Yoo*, J.-B. Yoon, KAIST, *National Nanofab Center

A nanoelectromechanical (NEM) switching device is developed with a new technique involving a liquid medium. Operation voltage is reduced by about 40% and the number of switching cycle with reliable device performance is improved dramatically, by more than 50 folds. The device has a 50 nm thick TiN cantilever with a 40 nm air-gap. A CMOS compatible process is employed.

Session 10: Emerging Technologies - Graphene Nanoelectronics

Tuesday, December 8, 9:00 a.m.
Holiday Ballrooms 1, 2 and 3
Chair: *Toshiro Hiramoto, University of Tokyo*

9:05 a.m.
10.1 Graphene for VLSI: FET and Interconnect Applications (Invited), Y. Awano, Keio University

Because of their remarkable physical properties, grapheme should be one of the most important Emerging Research Materials (ERM) for not only the front-end but also back-end devices of VLSIs for the next decade. In this paper, we discuss the present status of their material technologies and some issues to be addressed for realizing graphene channels and wiring devices for a future LSI.

9:30 a.m.
10.2 Development of Graphene FETs for High Frequency Electronics (Invited), Y.-M. Lin, K. Jenkins, D. Farmer, A. Valdes-Garcia, P. Avouris, C.-Y. Sung, H.-Y. Chiu, B. Ek, IBM

Recent advances in fabricating, measuring, and modeling of top-gated graphene FETs for high-frequency electronics are reviewed. By improving the oxide deposition process and reducing series resistance, an intrinsic cut-off frequency as high as 50 GHz is achieved in a 350-nm-gate graphene FET at a drain bias of 0.8 V. This fT value is the highest frequency reported to date for any graphene transistor, and it also exceeds that of Si MOSFETs at the same gate length illustrating the potential of grapheme for RF applications.

9:55 a.m.
10.3 Graphene Nanoribbon Devices and Quantum Heterojunction Devices (Invited), P. Kim, M.Y. Han, A.F. Young, I, Meric, K.C. Shepard, Columbia University

We fabricate lithographically patterned graphene nanoribbon structures. The sizes of these energy gaps estimated from the conductance in the nonlinear response regime indicate that the gap is scaling inversely proportional to the width of the ribbons. The temperature dependent conductance measurements suggest the substantial amount of edge disorders in the graphene nanoribbons. We also fabricate the lateral graphene heterojunction devices employing the local top gate structures. Quantum conductance oscillations are observed in these devices.

10:20 a.m.
10.4 Perspectives of Graphene Nanoelectronics: Probing Technological Options with Modeling (Invited), G. Iannaccone, G. Fiore, M. Macucci, P. Michetti, M. Micheli, A. Betti, P. Marconcini, University of Pisa

In this paper we show how numerical and analytical modeling of graphene-based devices is used to consider possible approaches to engineer a gap in graphene and to evaluate the perspectives of different technological options towards graphene nanoelectronics.

10:45 a.m.
10.5 Spin Transport in Single – and Multi Layer Graphene (Invited), M. Shiraishi, Osaka University, PRESTO-JST

In this talk, I present generation of a pure spin current, manipulation and unprecedented robustness of spin polarization of injected spins and gate-modulation of spin signals in single- and multi-layer graphene at room temperature, which can be important milestones for future graphene spin transistors.

11:10 a.m.
10.6 NEMS Application of Graphene, C. Chen, S. Rosenblatt, K.I. Bolotini, P. Kim, I. Kymissis, H.L. Stormer, T.F. Heinz J. Hone, Columbia University H.L. Stormer, T.F. Heinz

We have studied the mechanical properties of graphene and demonstrated its implementation in high-frequency NEMS resonators with electrical readout. To lay the foundation for applications such as mass sensing, we have modeled the response of the resonators and studied their response to changes is mass and temperature.

Session 11: Memory Technology – RAM and Modeling of Memory Reliability

Tuesday, December 8, 9:00 a.m.
Key Ballrooms 7, 9 and 10
Co-Chairs: *Rajeev Malik, IBM*
Daniele Ielmini, Politecnico di Milano

9:00 a.m.
Introduction

9:05 a.m.
11.1 Scaling Deep Trench Based eDRAM on SOI to 32nm and Beyond, G. Wang, D. Anand, N. Butt, A. Cestero, M. Chudzik, J. Ervin, S. Fang, G. Freeman, H. Ho, B. Khan, B. Kim, W. Kong, R. Krishnan, S. Krishnan, O. Kwon, J. Liu, K. McStay, E. Nelson, K. Nummy, P. Parries, J. Sim, R. Takalkar, A. Tessier, R. Todi, R. Malik, S. Stiffler, S.S. Iyer, IBM Semiconductor Research & Development Center

In this paper, we discuss scaling the deep trench eDRAM cell on SOI to simultaneously meet density, performance and retention requirements. We present this data for high performance deep trench based SOI eDRAM cells fabricated in 45nm and 32nm with a clear path to 22nm.

9:30 a.m.
11.2 Novel DRAM Cell with Amplified Capacitor for Embedded Application, H.-J. Cho, M.-R. Lin, GLOBALFOUNDRIES, Inc.

Novel DRAM cell with logic process compatible and whose memory operation is the same as the conventional DRAM operation is first time introduced. The cell uses the MOS capacitor with open base NPN bipolar transistor to amplify the storage capacitor. We fabricated the prototype cell and demonstrated the cell operation.

9:55 a.m.

11.3 Scalability of TiN/HfAlO/TiN MIM DRAM Capacitor to 0.7-nm-EOT and Beyond, N. Mise, O. Tonomura, T. Sekiguchi, S. Horii*, H. Itatani*, A. Ogawa*, T. Saito*, M. Sakai*, Y. Takebayashi*, H. Yamazaki*, K. Torii, Hitachi Ltd., *Hitachi Kokusai Electric Inc.

For screening materials for future MIM DRAM capacitors, we have theoretically investigated the tunneling barrier (current) as a function of permittivity, band offset and applied voltage at a fixed EOT and concluded that cubic-HfO_2 (HfAlO) with TiN is promising. We have also experimentally obtained 0.7-nm-EOT and 80 nA/cm^2 by TiN/HfAlO/TiN.

10:20 a.m.

11.4 RTS-like Fluctuation in Gate Induced Drain Leakage Current of Saddle-Fin Type DRAM Cell Transistor, H. Kim, K. Kim*, T.-K. Oh*, S.-Y. Cha*, S.-J. Hong*, S.-W. Park*, H. Shin, Seoul National University, Hynix Semiconductor

We investigated RTS-like fluctuation in GIDL current of Saddle-Fin (S-Fin) type DRAM cell transistor for the first time. Furthermore, two types of fluctuation which have apparently different τ_{high} to τ_{low} ratio were investigated, and it was found that the energy difference between bistable levels is similar to that of the junction leakage reported in [3] which is based on VO defect model.

10:45 a.m.
11.5 Atomistic Guiding Principles for MONOS-Type Memories with High Program/Erase Cycle Endurance,
K. Yamaguchi, A. Otake, K. Kobayashi, K. Shiraishi, University of Tsukuba

We have proposed atomistic guiding principles for high program/erase (P/E) cycle endurance MONOS type memories based on the first principles calculations. We have found that excess O atoms near SiN/SiO_2 interfaces are the cause of memory degradations due to its irreversible structural change during P/E cycles.

11:10 a.m.
11.6 45nm Low Power CMOS Logic Compatible Embedded STT MRAM Utilizing a Reverse-Connection 1T/1MTJ Cell, C.J. Lin, S.H. Kang*, Y.J. Wang, K. Lee*, X. Zhu*, W.C. Chen*, X. Li*, W.N. Hsu*, Y.C. Kao, M.T. Liu, W.C. Chen, Y.C. Lin, M. Nowak*, N. Yu*, L. Tran, TSMC, *Qualcomm Incorporated

This paper reports a 45nm spin-transfer-torque (STT) MRAM embedded into a standard CMOS logic platform that employs low-power (LP) transistors and Cu/LK BEOL. We believe that this is the first-ever demonstration of embedded STT MRAM that is fully compatible with the 45nm logic technology. To ensure the switching margin, a novel “reverse-connection” 1T/1MT cell has been developed with a cell size of 0.1026 μm^2. This cell is utilized to build embedded memory macros up to 32 Mbit in density. Device attributes and design windows have been examined by considering PVT variations to secure operating margins. Promising early reliability data on endurance, read disturb, and thermal stability have been obtained.

11:35 a.m.
11.7 A 0.5V Operation, 32% Lower Active Power, 42% Lower Leakage Current, Ferroelectric 6T-SRAM with V_{TH} Self-Adjusting Function for 60% Larger Static Noise Margin, S. Tanakamaru, T. Hatanaka, R. Yajima, M. Takahashi*, S. Sakai*, K. Takeuchi, University of Tokyo, *National Institute of Advanced Industrial Science and Technology

A ferroelectric 6T-SRAM is proposed. During the read/hold, VTH of ferroelectric transistors automatically changes to increase the static noise margin, SNM, by 60%. During the stand-by, VTH increases to decrease the leakage current by 42%. Enlarged SNM reduces the supply voltage by 0.11V, which decreases the active power by 32%.

Session 12: CMOS Devices and Technology – FinFET and Nanowire Devices

Tuesday, December 8, 9:00 a.m.
Key Ballrooms 8, 11 and 12
Co-Chairs: *Rusty Harris, Texas A&M*
Olivier Faynot, LETI
9:00 a.m.
Introduction

9:05 a.m.
12.1 Challenges and Solutions of FinFET Integration in an SRAM Cell and a Logic Circuit for 22 nm Node and Beyond (Invited), H. Kawasaki, V.S. Basker, T. Yamashita, C.-H. Lin*, Y. Zhu*, J. Faltermeier, S. Schmitz, J. Cummings, S. Kanakasabapathy, H. Adhikari**, H. Jagannathan, A. Kumar*, K. Maitra**, J. Wang, C.-C. Yeh, C. Wang*, M. Khater*, M. Guillorn*, N. Fuller*, J. Chang*, L. Chang*, R. Muralidhar*, A. Yagishita, R. Miller**, Q. Ouyang*, Y. Zhang*, V.K. Paruchuri, H. Bu, B. Doris, M. Takayanagi, W. Haensch*, D. McHerron, J. O'Neill, K. Ishimaru, Toshiba America Electronic Components Inc. & IBM Research at Albany Nanotech, *IBM TJ Watson Research Center, **GLOBALFOUNDRIES Inc.

FinFET integration challenges and solutions are discussed. Fin dimension scaling is presented for future technology nodes. Challenges for 3-D structures are reviewed for SRAM cell scaling. Rpara reduction is discussed for a logic FinFET. The proposed diamond-shape epi structure will be effective for future FinFET technologies.

9:30 a.m.
12.2 A 25-nm Gate-Length FinFET Transistor Module for 32nm Node, C.-Y. Chang, T.-L. Lee, C. Wann, L.-S. Lai, H.-M. Chen, C.-C. Yeh, C.-S. Chang, C.-C. Ho, J.C. Sheu, T.M. Kwok, F. Yuan, S.M. Yu, C.F. Hu, J.J. Shen, Y.H. Liu, C.P. Chen, S.-C. Chen, L.S. Chen, L. Chen, Y.H. Chiu, C.-Y. Fu, M.J. Huang, Y.-L. Huang, S. Hung, J.J. Liaw, H.C. Lin, H.H. Lin, L.-T.S. Lin, S.S. Lin, Y.J. Mii, E. Ou-Yang, M.F. Shieh, C.C. Su, S.P. Tai, H.J. Tao, M.H. Tsai, K.-T. Tseng, K.W. Wang, S.B. Wang, J.J. Xu, F.-K. Yang, S.-T. YangC.N. Yeh, TSMC

We present a high-performance and low-power FinFET module at 25 nm gate length. When normalized to the actual fin perimeter, N-FinFET and P-FinFET have 1200 and 915 uA/um drive current respectively at 100nA/um leakage under 1V. To our knowledge this is the best FinFET drive current at such scaled gate length.

9:55 a.m.
12.3 High Performance and Highly Uniform Gate-All-Around Silicon Nanowire MOSFETs with Wire Size Dependent Scaling, S. Bangsaruntip, G.M. Cohen, A. Majumdar, Y. Zhang, S.U. Engelmann, N.C.M. Fuller, L.M. Gignac, S. Mittal, J.S. Newbury, M. Guillorn, T. Barwicz, L. Sekaric, M.M. Frank, J.W. Sleight, IBM TJ Watson Research Center

We demonstrate undoped-body gate-all-around (GAA) Si nanowire (NW) MOSFETs with excellent electrostatic scaling. These NW devices, with TaN/Hf-based gate stack, have high drive-current performance with NFET/PFET I_{DSAT} = 2600/2920 µA/µm at supply voltage V_{DD} = 1 V and off-current I_{OFF} = 15-30 nA/µm. Superior NW uniformity is obtained through the use of a combined hydrogen annealing and oxidation process. Clear scaling of short channel effects versus wire size is observed.

10:20 a.m.

12.4 Demonstration of Scaled 0.099µm^2 FinFET 6T-SRAM Cell using Full-Field EUV Lithography for (Sub-) 22nm Node Single-Patterning Technology, A. Veloso, S. Demuynck, M. Ercken, A.M. Goethals, S. Locorotondo, F. Lazzarino, E. Altamirano, C. Huffman, A. De Keersgieter, S. Brus, M. Demand, H. Struyf, J. De Backer, J. Hermans, C. Delvaux, B. Baudemprez, T. Vandeweyer, F. Van Roey, C. Baerts, D. Goossens, H. Dekkers, P. Ong, N. Heylen, K. Kellens, H. Volders, A. Hikavyy, C. Vrancken, M. Rakowski, S. Verhaegen, M. Dusa*, L. Romijn*, C. Pigneret*, A. Van Dijk*, R. Schreutelkamp**, A. Cockburn**, V. Gravey**, H. Meiling*, B. Hultermans*, S. Lok*, K. Shah**, R. Rajagopalan**, J. Gelatos**, O. Richard, H. Bender, G. Vandenberghe, G. P. Beyer, P. Absil, T. Hoffmann, K. Ronse, S. Biesemans, IMEC, *ASML, **Applied Materials

We demonstrate functional 0.099um^2 6T-SRAM cells using full-field EUV lithography for contact and M1 levels and single-patterning. Key enablers include: 1) HK/MG FinFETs with 40nm Lg, 12-17nm wide Fins, and cell beta ratio of 1.3; 2) option for using an extension-less approach, with 2 less I/I photos, and enabling defect-free growth of Si-epitaxial raised S/D; 3) double thin-spacers and ultra-thin silicide; 4) optimized W metallization for high aspect-ratio, >=30nm-wide contacts. SRAM cell with SNM>0.1VDD down to 0.4V, and healthy cell transistors [SS~80mV/dec, DIBL~50-80mV/V, $|V_{Tlin}| \leq 0.2$V (PMOS), V_{Tlin}~0.36V (NMOS)] are reported.

10:45 a.m.

12.5 Experimental Assessment of Self-Heating in SOI FinFETs, A.J. Scholten, G.D.J. Smit, R.M.T. Pijper, L.F. Tiemeijer, H.P. Tuinhout, J.-L.P.J. van der Steen*, A. Mercha**[‡], M. Braccioli, D.B.M. Klaassen, NXP-TSMC Research Centre, *Universiteit Twente, **IMEC, [‡]University of Bologna

We have demonstrated a gigantic effect of self-heating on capacitances and used it to extract the thermal impedance of SOI FinFETs. We show that, although the effect of self-heating on the FinFET on-current is modest, the associated temperature rise is very significant. The method can be used directly on measured data, and is therefore a valuable tool for FinFET technology development.

11:10 a.m.

12.6 Dual Channel FinFETs as a Single High-k/Metal Gate Solution Beyond 22nm Node, C.E. Smith, H. Adhikari*, S-H. Lee, B. Coss, S. Parthasarathy, C. Young, B. Sassman, M. Cruz, C. Hobbs, P. Majhi, P.D. Kirsch, R. Jammy, SEMATECH, *GLOBALFOUNDRIES

We report the promise of dual channel materials using FinFETs for high-performance CMOS for sub 22 nm technology node. pFinFETs with SiGe channel on insulator (SiGeOI) fabricated using standard cMOS processing exhibit 3.6X hole mobility enhancement over Silicon(100) while allowing for VTH control with single high-k and metal gate stack.

11:35 a.m.

12.7 Relationship Between Mobility and High-k Interface Properties in Advanced Si and SiGe Nanowires, K. Tachi, M. Casse, D. Jang*, C. Dupre, A. Hubert, N. Vulliet**, C. Maffini-Alvaro, C. Vizioz, C. Carabasse, V. Delaye, J.M. Hartmann, G. Ghibaudo*, H. Iwai^, S. Cristoloveanu*, O. Faynot, T. Ernst, CEA-LETI MINATEC, *IMEP-LAHC, INPG-MINATEC,**STMicroelectronics, ^Tokyo Institute of Technology

For the first time, interface properties between high-k and Si nanowires (NWs) have been experimentally investigated by adapting charge pumping technique. It is found that the interface state density of circular Si NWs is higher than that of rectangular ones. The trap densities are well correlated to with the mobility.

Session 13: Quantum, Power, and Compound Semiconductors – III-V Logic Transistors with Advanced Gate Stack

Tuesday, December 8, 9:00 a.m.
Key Ballrooms 3 and 4
Co-Chairs: Suman Datta, Pennsylvania State University
Jan Sonsky, NXP Semiconductors

9:00 a.m.
Introduction

9:05 a.m.
13.1 Advanced High-K Gate Dielectric for High-Performance Short-Channel $In_{0.7}Ga_{0.3}As$ Quantum Well Field Effect Transistors on Silicon Substrate for Low Power Logic Applications, M. Radosavljevic, B. Chu-Kung, S. Corcoran, G. Dewey, M.K. Hudait, J.M. Fastenau*, J. Kavalieros, W.K. Liu*, D. Lubyshev*, M. Metz, K. Millard, M. Makherjee, W. Rachmady, U. Shah, R. Chau, Intel Corporation, *IQE Inc.

An advanced composite high-K gate stack (4nm TaSiOx-2nm InP) has been integrated in the $In_{0.7}Ga_{0.3}As$ QWFET on silicon substrate to enable (i) both thin electrical oxide thickness, tOXE and low gate leakage, JG and (ii) effective carrier confinement and high effective carrier velocity, Veff in the QW channel.

9:30 a.m.
13.2 High-Performance Deep-Submicron Inversion-Mode InGaAs MOSFETs with Maximum G_m Exceeding 1.1 mS/μm:New HBr Pretreatment and Channel Engineering, Y.Q. Wu, M. Xu, R. Wang, O. Koybasi, P.D. Ye, Purdue University

We report deep-submicron inversion-mode NMOSFETs on $In_{0.7}Ga_{0.3}As$ using 2.5nm-5.0nm ALD Al_2O_3 as high-k gate dielectrics with Gm exceeding 1.1-1.3 mS/μm. The record Gm is about 50-75% larger than the values reported previously. Retro-grade structure and halo-implantation are first time introduced to III-V MOSFET field to improve the off-state performance of InGaAs MOSFETs.

9:55 a.m.
13.3 Enabling the High-Performance InGaAs/Ge CMOS: A Common Gate Stack Solution, D. Lin, G. Brammertz, S. Sioncke, C. Fleischmann, A. Delabie, K. Martens, H. Bender, T. Conard, W.H. Tseng**, J.C. Lin**, W.E. Wang, K. Temst*, A. Vatomme*, J. Mitard, M. Caymax, M. Meuris, M. Heyns, T. Hoffmann, IMEC, *KU Leuven, **TSMC

To address the integration of the high-mobility MOSFET, a common gate stack (CGS) approach is proposed for the first time and demonstrated on high performance transistors. Based on the duality found on the InGaAs/Ge MOS system, this approach aims to integrate the InGaAs/Ge MOSFET processes for high performance CMOS applications with an emphasis on progressive EOT scaling.

10:20 a.m.
13.4 First Experimental Demonstration of 100 nm Inversion-mode InGaAs FinFET Through Damage-Free Sidewall Etching, Y.Q. Wu, R. Wang, T. Shen, J.J. Gu, P.D. Ye, Purdue University

We report for the first experimental demonstration of inversion-mode $In_{0.53}Ga_{0.37}As$ tri-gate FinFET using damage-free etching process and ALD Al_2O_3 as gate dielectric. The SCE is greatly suppressed in terms of subthreshold slope (SS), drain induced barrier lowering (DIBL) and threshold voltage (VT) roll-off. Detailed analysis and comparison are performed on the FinFETs with channel length (Lch) from 200 nm to 100 nm, fin width (WFin) from 100 nm to 40 nm and the fixed fin height (HFin) of 40 nm.

10:45 a.m.

13.5 InGaAs MOSFET Performance and Reliability Improvement by Simultaneous Reduction of Oxide and Interface Charge in ALD (La)AlOx/ZrO_2 Gate Stack, J. Huang, N. Goel, H. Zhao[a], C. Y. Kang, K.S. Min, G. Bersuker, S. Oktyabrsky[b], C.K. Gaspe[c], M.B. Santos[c], P. Majhi, P.D. Kirsch, H.-H. Tseng[d], J.C. Lee[a], R. Jammy, SEMATECH, [a]University of Texas at Austin, [b]Suny-Albany, [c]University of Oklahoma, [d]Texas State University

The performance and reliability of $ZrO_2/In_{0.53}Ga_{0.47}As$ MOSFETs are shown to be improved by simultaneous reduction of dielectric and interface charges. An amorphous (La)AlOx interlayer at the $ZrO_2/In_{0.53}Ga_{0.47}As$ interface is a key to reduce border traps, interface traps and move ZrO_2 fixed charge away from the $In_{0.53}Ga_{0.47}As$.

11:10 a.m.

13.6 Thermally Robust Phosphorous Nitride Interface Passivation for InGaAs Self-Aligned Gate-First n-MOSFET Integrated with High-k Dielectric, H.-J. Oh, J. Lin, S.A.B. Suleiman, G.Q. Lo*, D.L. Kwong*, D.Z. Chi**, S.J. Lee, National University of Singapore, *Institute of Microelectronics, **Institute of Materials Research and Engineering

Plasma-based PH_3 passivation technique is extensively studied for high-k gate stack passivation on InGaAs substrate and comparative analysis reveals that the striking passivation improvement comes from a stable covalent-bond PxNy layer formation. PxNy passivation layer improves thermal stability of high-k gate stack on InGaAs up to 750°C, which enables successful implementation of self-aligned gate-first process InGaAs MOSFETs. By adopting P_xN_y passivation on InGaAs with MOCVD high-k and metal gate stack, we report the record G_m=378mS/mm at V_d=1V and effective mobility of 2557 cm^2/Vs at E_{eff}=0.24MV/cm.

11:35 a.m.

13.7 Experimental Demonstration of 100nm Channel Length $In_{0.53}Ga_{0.47}As$-based Vertical Inter-band Tunnel Field Effect Transistors (TFETs) for Ultra Low-Power Logic and SRAM Applications (Late News), S. Mookerjea, D. Mohata, R. Krishnan, J. Singh, A. Vallett, A. Ali, T. Mayer, V. Narayanan, D. Schlom*, A. Liu** and S. Datta, The Pennsylvania State University, *Cornell University, ** IQE Inc.

Vertical $In_{0.53}Ga_{0.47}As$ tunnel FETs with 100nm channel length and high-k/metal gate stack are demonstrated with high I_{on}/I_{off} ratio (>104). At VDS = 0.75V, a record on-current of 20μA/μm is achieved due to higher tunneling rate in narrow tunnel gap $In_{0.53}Ga_{0.47}As$.. The TFETs exhibit gate bias dependent NDR characteristics at room temperature under forward bias confirming band to band tunneling. The measured data are in excellent agreement with numerical simulation at all drain biases. A novel 6T TFET SRAM cell using virtual ground assist is demonstrated despite the asymmetric source/drain configuration of TFETs.

Session 14: Process Technology – Advanced 3D Technology and Processing

Tuesday, December 8, 9:00 a.m.
Key Ballroom 6
Co-Chairs: *Xiaomeng Chen, IBM*
Kyoungsub Shin, Samsung

9:00 a.m.
Introduction

9:05 a.m.

14.1 Advances in 3D CMOS Sequential Integration, P. Batude, M. Vinet, A. Pouydebasque, C. Le Royer, B. Previtali, C. Tabone, J.-M. Hartmann, L. Sanchez, L. Baud, V. Carron, A. Toffoli, F. Allain, V. Mazzocchi, D. Lafond, O. Thomas, O. Cueto, N. Bouzadia, D. Fleury**, A. Amara*, S. Deleonibus, O. Faynot, CEA LETI MINATEC, *ISEP, **STMicroelectronics

For the first time, 3D sequential CMOS integration turns up to be an actual competitor for sub 22nm technology nodes. Thanks to the original use of molecular bonding, high quality top Si active layer are obtained. Thermally robust bottom salicide goes through the whole top FET process without any significant sheet resistance degradation. The low temperature integration of raised source and drain for top layers is demonstrated. A decrease by 4Å of the Equivalent Oxide Thickness is measured when low thermal budget process is implemented. The electrostatic coupling between stacked FETs is demonstrated thanks to ultra thin inter layer dielectric thickness of 60nm. It leads to a threshold voltage shift of 130mV enabling SRAM stabilization.

9:30 a.m.
14.2 Three-Dimensional Integration Technology Based on Reconfigured Wafer-to-Wafer and Multichip-to-Wafer Stacking Using Self-Assembly Method, T. Fukushima, E. Iwata, Y. Ohara, A. Noriki, K. Framura, K.-W. Lee, J. Bea, T. Tanaka, M. Koyanagi, Tohoku University

We demonstrated new 3D integration using reconfigured and direct self-assembled multichip-to-wafer stacking . In these 3D integration, key technologies of liquid pull-down, selective hydrophilzing, and super hydrophobic technologies were developed. High alignment accuracy of 200 nm was obtained by the self-assembly with water. Furthermore, chips with microbumps were successfully self-assembled and directly bonded without thermal compression. They showed good electrical characteristics.

9:55 a.m.
14.3 Enabling 3D-IC Foundry Technologies for 28 nm Node and Beyond: Through-Silicon-Via Integration with High Throughput Die-to-Wafer Stacking, D.Y. Chen, W.C. Chiou, M.F. Chen, T.D. Wang, K.M. Ching, H.J. Tu, W.J. Wu, C.L. Yu, K.F. Yang, H.B. Chang, M.H. Tseng, C.W. Hsiao, Y.J. Lu, H.P. Hu, Y.C. Lin, C.S. Hsu, W.S. Shue, C.H. Yu, TSMC

High density through-silicon-via and cost-effective 3D die-to-wafer integration scheme are proposed as foundry solutions for CMOS chips at 28 nm node and beyond. Key processes include: TSV formation, extreme thinning and die-to-wafer assembly. The impact of extreme thinning on device Vth,sat, leakage, and Ion-Ioff characteristics of bulk CMOS devices with and without e-SiGe/CESL stressors has been minimized. The presence of TSV caused no significant degradation in Cu/ELK reliability. These excellent characteristics suggest the 3D-IC processes are promising and suitable for adoption in next generation integrated circuits and interconnects.

10:20 a.m.

14.4 3D Stacked ICs Using Cu TSVs and Die to Wafer Hybrid Collective Bonding, G. Katti , A. Mercha, J. Van Olmen , C. Huyghebaert, A. Jourdain, M. Stucchi, M. Rakowski, I. Debusschere, P. Soussan, W. Dehaene, K. De Meyer, Y. Travaly, E. Beyne, S. Biesemans, B. Swinnen, IMEC, KU Leuven

We report 3D circuits obtained by a 3D Stacked IC approach using both Cu through Silicon Vias (TSV) First and Die-to-Wafer Hybrid Collective bonding. The CMOS devices integrity and a lumped RC TSV models are also validated through model hardware correlation using 3D RO with inverters on top tiers and bottom wafer alternatively connected through 40 TSVs.

10:45 a.m.

14.5 Impact of Remnant Stress/Strain and Metal Contamination in 3D-LSIs with Through-Si Vias Fabricated by Wafer Thinning and Bonding, M. Murugesan, J.C. Bea, H. Kino, Y. Ohara, T. Kojima, A. Noriki, K.W. Lee, K. Kiyoyama, T. Fukushima, H. Nohira, T. Hattori, E. Ikenaga*, T. Tanaka, M. Koyanagi, Tohoku University, *JASRI

The remnant stress due to wafer thinning process in extremely thin (10 micron) Si wafers was investigated by micro-Raman Spectroscopy andX-ray Photo Electron Spectroscopy, and the data revealed that chmical mechanical polishing method was the best among all the stress relieving method studied. From the electrical characteristics of n- and p-MOSFET, we have deduced a 3% change in the ON current ratio when the 50 micron thick wafer subjected to bend few microns. The deleterious role of inevitable metal contamination on the device performance was studied by determining the minority-carrier-life- time in MOS capacitor after accelerated diffusion with Cu.

11:10 a.m.
14.6 Ultra Thinning 300-mm Wafer Down to 7-µm for 3D Wafer Integration on 45-nm Node CMOS using Strained Silicon and Cu/Low-k Interconnects, Y. S. Kim, A. Tsukune, N. Maeda*, H. Kitada*, A. Kawai**, K. Arai**, K. Fujimoto^, K. Suzuki^, Y. Mizushima^^, T. Nakamura^^, T. Ohba*, T. Futatsugi, M. Miyajima, Fujitsu Microelectronics Limited, *University of Tokyo, **DISCO Corporation, ^Dai Nippon Printing, ^^Fujitsu Laboratories Ltd.

High performance 45-nm Node and its 3D integration employed aggressively thinned down to 7-µm of 300-mm wafer for the Wafer-on-a-Wafer (WOW) application has been succeeded for the first time. The impact of ultra thin wafer on strained transistors and Cu/low-k multilevel interconnects is described, and no degradation regarding electrical performance is found.

Session 15: Displays, Sensors and MEMS – Organic Electronics

Tuesday, December 8, 9:00 a.m.
Key Ballroom 5
Co-Chairs: *Karlheinz Bock, University of Berlin*
Hiroaki Fujita, Eastman Kodak

9:00 a.m.
Introduction

9:05 a.m.
15.1 Thin-Film Transistors and Circuits on Plastic Foil (Invited), P. Heremans, J. Genoe, S. Steudel, K. Myny, S. Smout, P. Vicca, C. Grillberger**, O. Hild**, F. Furthner*, B. van der Putten*, A.K. Tripathi*, G.H. Gelinck*, IMEC, *TNO-Holst Centre, **Fraunhofer Institute of Photonic Microsystems, KU LEuven

We present our recent achievements in organic semiconductor technology in two emerging application areas. We show that the performance of our technology approaches the requirements for Electronic Product Coding RFID tags. Also, backplanes of OLED displays are enabled by the unique compatibility of pentacene transistors with high-k gate dielectrics.

9:30 a.m.

15.2 A 1-V Operated Polymer Vertical Transistor with High On/Off Current Ratio, Y.-C. Chao, W.-W. Tsai, C.-Y. Cheng, H.-W. Zan, H.-F. Meng, S.-L. Jiang, C.-M. Chiang, M.-C. Ku, National Chiao Tung University

A 1-V solution-processed polymer vertical transistor with on/off current ratio higher than $2x10^4$ is firstly demonstrated. Significant impacts of thin film morphology and metal doping effect on the leakage current of transistors are firstly observed. The complete leakage control and the reliable process enable polymer vertical transistors for real applications.

9:55 a.m.

15.3 Fermi Level Depinning at Metal-Organic Semiconductor Interface for Low-Resistance Ohmic Contacts, Z. Liu, M. Kobayashi, B.C. Paul, Z. Bao, Y. Nishi, Stanford University, Toshiba

This paper presents, for the first time, the successful demonstration of Fermi-level depinning at M/O interface by inserting a precisely-controlled ultrathin interfacial Si_3N_4 insulator. The contact behavior is successfully tuned from rectifying to ohmic and to tunneling by modulation of the Si_3N_4 thickness within 0-6 nm. Detailed physical mechanisms of Fermi-level pinning/depinning responsible for the M/O contact resistance behavior are also clarified based on a proposed dipole model.

10:20 a.m.
15.4 Dual Threshold Voltage Integrated Organic Technology for Ultralow-Power Circuits, I. Nausieda, K. Ryu, D.D. He, A.I. Akinwande, V. Bulovic, C.G. Sodini, Massachusetts Institute of Technology

A dual threshold voltage (VT) organic thin-film transistor technology for large-area flexible integrated circuits is presented. Two VTs are enabled by using different gate metals. Fabricated inverters and rail-to-rail ring oscillators function at 3V VDD and consume picowatts. The availability of two VTs reduces inverter area by 30x and increases speed by 17x.

10:45 a.m.
15.5 Vertical Transport in Spin Coated Ultra Thin Polycrystalline Pentacene Organic Stacks, S. Altazin, R. Clerc*, R. Gwoziecki, D. Boudinet, J. M. Verilhac, R. Coppard, G. Ghibaudo*, G. Pananakakis*, C. Serbutoviez, LITEN CEA, *IMEP-LAHC

Experiments and modeling have been used to investigate the transport in vertical spin coated TIPS-pentacene layers used in rectifying diodes. It has been shown that the vertical transport properties are not as good as the longitudinal one, due to the particular nature of the polycrystalline film obtained by this process.

11:10 a.m.
15.6 All Inkjet Printed Self-Aligned Transistors and Circuits Applications, H.-Y. Tseng, V. Subramanian, University of California, Berkeley

We fabricate devices and circuit blocks using a novel, fully-printed transistor process that self-aligns source/drain electrodes to gates, resulting in improved overlap capacitance. These are used with a self-aligned interconnect to realize fully-printed transistor arrays and inverters showing performance suitable for use in a range of low-cost electronics applications

Session 16: Characterization, Reliability and Yield – Product Reliability and ESD

Tuesday, December 8, 9:00 a.m.
Key Ballrooms 1 and 2
Co-Chairs: *Srikanth Krishnan, Texas Instruments*
Elyse Rosenbaum, University of Illinois at Urbana-Champaign

9:00 a.m.
Introduction

9:05 a.m.
16.1 A Viable and Comprehensive TDDB Assessment Methodology for Investigation of SRAM V_{min} Failure, E. Wu, G. Braceras, D. Turner, A. Swift, M. Johnson, J. Suñé*, S. Tous*, B. Li, R. Bolam, G. Massey, M. Khare**, IBM System and Technology Group, *Universitat Autonoma de Barcelona, **IBM SRDC

For the first time, we show the fundamental breakdown physics such as power-law voltage acceleration model and progressive breakdown methodology can lead us to successfully explain SRAM Vmin failure, thus a viable TDDB assessment methodology can be established.

9:30 a.m.
16.2 Impact of Transistor Reliability on RF Oscillator Phase Noise Degradation, V. Reddy, N. Barton, S. Martin, C. M. Hung, A. Krishnan, C. Chancellor, S. Sundar, A. Tsao, D. Corum, N. Yanduru, S. Madhavi, S. Akhtar, N. Pathak, P. Srinivasan, S. Shichijo, K. Benaissa, A. Roy, T. Chatterjee, R. Taylor, J. Krick, J. Brighton, J. Ondrusek, D. Barry, S. Krishnan, Texas Instruments

The impact of deep sub-micron CMOS transistor reliability on RF oscillator phase noise degradation is demonstrated along with the importance of off-state drain stress for large signal RF applications. Process and device optimization was successful in reducing phase noise degradation to acceptable levels.

9:55 a.m.
16.3 Technologies to Further Reduce Soft Error Susceptibility in SOI, P. Oldiges, R. Dennard*, D. Heidel*, T. Ning*, K. Rodbell*, H. Tang*, M. Gordon*, L. Wissel, IBM Corporation, *IBM Research

Methods for soft error rate reduction in silicon on insulator devices and circuits are explored and evaluated via simulations that have been validated against hardware measurements. Our methodology is first introduced, and the followingg techniques are examined in detail: 1) Body thinning, 2) carrier G/R lifetime reduction, 3) body contacts, 4) stacked devices, 5) parallel devices. Finally, the advantages and disadvantages of all methods are described.

10:20 a.m.
16.4 Multiscale Modeling for Reliability Assessment in Microelectronic Systems (Invited), K. Mysore, G. Subbarayan, Purdue University

In this paper, we discuss challenges to modeling reliability in microelectronic systems wherein issues generically involve evolving heterogeneities such as cracks, voids, and secondary phases occur across all relevant length scales starting from the circuit board down to the Inter-Layer Dielectric (ILD). Increasingly the failures at ILD length scales are driven by package construction or material choices such as the underfill stiffness. Thus, often, a complex combination of material, geometry, and loading together determine whether local (such as a specific ILD layer or via location) or global (such as a package solder balls or underfill) failures occur preferentially. In this paper we describe several examples of reliability modeling from our recent research spanning both the package-level and die-level reliability issues.

10:45 a.m.
16.5 Impact of Strain Engineering and Channel Orientation on the ESD Performance of Nanometer Scale CMOS Devices, J. Lu, C. Duvvury*, H. Gossner**, K. Banerjee, University of California, Santa Barbara, *Texas Instruments Inc., **Infineon Technologies AG

This paper provides the first insights into the effect of strain engineering on ESD performance for nano-scale ggNMOS and ggPMOS protection devices by coupling electro-thermal simulations with tight-binding band structure calculation, mobility modeling and thermal conductivity evaluation. The preferential stress and channel orientations for both ggNMOS and ggPMOS are also proposed for the first time.

11:10 a.m.
16.6 Filament Study of STI Type Drain Extended NMOS Device using Transient Interferometric Mapping, M. Shrivastava, S. Bychikhin*, D. Pogany*, J. Schneider**, M.S. Baghini, H. Gossner**, E. Gornik*, V.R. Rao, Indian Institute of Technology-Bombay, *Vienna University of Technology, **Infineon Technologies AG

We present the filament behavior of STI type DeNMOS devices under ESD conditions by using detailed Transient Interferometric Mapping experiments and 3D TCAD simulations. Various events during current filamentation are explored. By uniform turn-on of the device during base push-out the failure current could be improved by more than 2X.

Session 17: Process Technology – High-k and Metal Gate Technology

Tuesday, December 8, 2:15 p.m.
Holiday Ballrooms 1, 2 and 3
Co-Chairs: *Weng Chang, Taiwan Semiconductor Manufacturing Company Ltd.*
Yoshinori Tsuchiya, Toshiba America Electronic Components Inc.

2:15 p.m.
Introduction

2:20 p.m.
17.1 Understanding Mobility Mechanisms in Extremely Scaled HfO_2 (EOT 0.42 nm) Using Remote Interfacial Layer Scavenging Technique and V_t-tuning Dipoles with Gate-First Process, T. Ando, M.M. Frank, K. Choi*, C. Choi, J. Bruley, M. Hopstaken, M. Copel, E. Cartier, A. Kerber*, A. Callegari, D. Lacey, S. Brown, Q. Yang, V. Narayanan, IBM TJ Watson Research Center, *GLOBALFOUNDRIES

We demonstrate a novel remote interfacial layer (IL) scavenging technique yielding a record-setting EOT (0.42 nm) for HfO_2. Intrinsic IL scaling effects are clarified using this method. The remote IL scavenging combined with La enables Vt control and EOT scaling meeting the 16 nm node requirements without extrinsic mobility degradation.

2:45 p.m.
17.2 Ti-capping Technique as a Breakthrough for Achieving Low Threshold Voltage, High Mobility, and High Reliability of pMOSFET with Metal Gate and High-k Dielectrics Technologies, H. Takahashi, H. Minakata, Y. Morisaki, S. Xiao, M. Nakabayashi, K. Nishigaya, T. Sakoda, K. Ikeda, H. Morioka, N. Tamura, M. Kase, Y. Nara, Fujitsu Microelectronics Ltd.

We proposed inhibition mechanism of common Al-capping technique in pMOSFET V_{th} control for the first time, and established effective Ti-capping technique using metal gate and Hf-based high-*k* dielectrics. Ti-capping technique can adjust lower V_{th} than Al capping without the degradation of mobility and NBTI.

3:10 p.m.
17.3 V_{th} Fluctuation Suppression and High Performance of HfSiON/Metal Gate Stacks by Controlling Capping-Y_2O_3 Layers for 22nm Bulk Devices, S. Kamiyama, E. Kurosawa, S. Abe, M. Kitajima, T. Aminaka, T. Aoyama, K. Ikeda, Y. Ohji, Selete

We have succeeded that random threshold-voltage fluctuations are suppressed to control capping-layers and high-k-materials with metal-gate-first-stacks for 22-nm-node devices. By employing 1-2ML Y_2O_3-layers on HfSiON films, V_{th} fluctuations are the same for non-capping-samples in spite of excellent V_{th} controllability ($|\Delta Vth|>180mV$). Furthermore, those have high device-performance because ultra-thin-equivalent-oxide-thickness (0.74nm) can be achieved with high electron-carrier-mobility, and very high drain-current ($I_{on}>1060\mu A/\mu m$).

3:35 p.m.

17.4 A Novel Damage-Free High-k Etch Technique Using Neutral Beam-Assisted Atomic Layer Etching (NBALE) for Sub-32nm Technology Node Low Power Metal Gate/High-k Dielectric CMOSFETs, K.S. Min, C.Y. Kang, C. Park, C.S. Park, B.J. Park*, J.B. Park*, M.M. Hussain, J.C. Lee**, B.H. Lee^, P. Kirsch, H-H. Tseng, R. Jammy, G.Y. Yeom*, SEMATECH, *Sungkyunkwan University, **University of Texas at Austin, ^Gwangju Institute of Science and Technology

For the first time, a novel damage-free neutral beam-based atomic etching process has successfully demonstrated the removal of the residual high-k dielectric layer after gate patterning. Due to its neutralized atomic flux and chemical reaction, high etch selectivity are observed resulting in improved device performance and reliability. This process would enhance the high-K/metal gate manufacturability significantly.

4:00 p.m.

17.5 Engineering the Complete MANOS-type NVM Stack for Best in Class Retention Performance, D.C. Gilmer, N. Goel, H. Park, C. Park, S. Verma*, G. Bersuker, P. Lysaght, H.-H. Tseng**, P.D. Kirsch, K.C. Saraswat, R. Jammy, SEMATECH, *Stanford University, **Texas State University, San Marco

High performance MANOS demonstrated through improved P/E, endurance and retention. Band-engineered tunnel-oxide and SiNx trap can optimize P/E, and endurance with trade-off in retention. However, combining these techniques with band-engineered blocking layer and oxygen-bearing high EWF electrode can improve retention while maintaining the benefits of engineering each individual stack component.

Session 18: 2009 IEDM Special Session: Confluence of Technology and Design: Design Issues on 32/22nm and Beyond

Tuesday, December 8, 2:15 p.m.
Key Ballrooms 7, 9 and 10
Chair: Meikei Ieong, TSMC

Recognizing the increasing importance of the inter-dependence of circuit and technology, the IEDM started a special all-invited session on the confluence of design and process technology back in 2007. This year's theme is "Design Issues in Advanced CMOS Technology". This session brings together design experts from different application areas to discuss issues in advanced CMOS nodes, such as 32, 22, and 15nm nodes.

2:15 p.m.
Introduction

2:20 p.m.
18.1 Beyond Innovation: Dealing with the Risks and Complexity of Processor Design in 22nm (Invited), Carl Anderson, IBM

Current and future Si technologies allow microprocessor designs to contain billions of transistors. Design tool and methodology improvements have allowed designers to implement microprocessors that have exponentially grown to billions of transistors with design teams that have only modest growth in size. Innovations have allowed technology feature sizes to scale to almost tenth of the wave length of light used to define them. This has added significant complexity to the technology and designs. This paper discusses the importance of discipline and risk management in the design of new high performance microprocessors in advanced technologies. Innovation is very important in these designs but the design costs have to be assessed and the risks managed.

2:45 p.m.
18.2 Design Challenges for 22nm CMOS and Beyond" (Invited), S. Borkar, Intel

This paper presents technology and economic challenges posed by 22nm CMOS and beyond. They can be addressed by advances in design technology, methodology, validation, and testing, to continue to enjoy the benefits of CMOS scaling in the future, as we have over the past decades.

3:10 p.m.
18.3 Analog and RF Design Issues in High-k and Multi-Gate CMOS Technologies (Invited), M. Fulde, D. Schmitt-Landsiedel* and G. Knoblinger, Infineon, *Technical University Munich

High-k, metal gate devices and furthermore multi-gate FETs (MuGFETs) are considered as promising solution for scaling down to 32nm, 22nm and 16nm overcoming the limitations of conventional planar bulk. Especially analog, mixed-signal and RF device and circuit performance is affected by these revolutionary changes in technology. This paper discusses different examples for novel, technology related design issues focused on analog, mixed-signal and RF applications.

3:35 p.m.
18.4 Design Issues and Possible Solutions for Low Cost and High Efficiency LSIs (Invited), M. Mizuno, NEC Electronics

Large scale integration with advanced CMOS technologies has been reducing cost, but maintaining chip dependability is becoming more and more difficult. This is due to increasing complexity of system design and increasing uncertainty of signal timing and level. Chip dependability can be realized at low cost and maintain high efficiency by combining technologies of (A) "Never produce defects" during chip design and manufacturing, (B) "Never let defects escape" during chip testing, and (C) "Never let defects lead to failure" during operations, as shown in Fig. 1.

4:00 p.m.
18.5 Design and Process Co-optimization for 28nm/22nm and Beyond - A Foundry's Perspective (Invited), C. Hou, TSMC

This paper presents challenges in the advanced process technologies, and the need to adopt a new collaboration model between the designer and the foundry.

4:25 p.m.
18.6 Co-optimizing Process Development, Layout and Circuit Design for Cost-Effective 22nm Technology Platform (Invited), K. Michaels, PDF Solutions

The economic and technological challenges of process development are threatening the timely availability of advanced nodes. Meanwhile design and product organizations are demanding the continued delivery of Moore’s law density scaling to justify node migration. Balancing the requirements of design with the capabilities and physical limitations of advanced processes will require capitalizing on opportunities for co-optimization between process development, layout and circuit design. In this presentation, we will examine the challenges and highlight the opportunities for achieving an economically feasible path to 22nm.

Session 19: CMOS Devices and Technology – Channel Transport in Advanced Si and Ge Devices

Tuesday, December 8, 2:15 p.m.
Key Ballrooms 8, 11 and 12
Co-Chairs: *Luca Selmi, University of Udine*
Ken Rim, IBM SRDC

2:15 p.m.
Introduction

2:20 p.m.
19.1 Experimental Demonstration of High Mobility Ge NMOS, D. Kuzum, T. Krishnamohan*, A. Nainani, Y. Sun, P.A. Pianetta, H.S-.P. Wong, K.C. Saraswat, Stanford University, *also with Intel

We demonstrate the highest electron mobility for Ge NMOS to-date, greater than 1.5 X of universal Si mobility. Detailed interface characterizations, trapping analyses and gated Hall MOSFET measurements are performed to identify the main mechanisms behind poor Ge NMOS performance in the past.

2:45 p.m.
19.2 Record-high Electron Mobility in Ge n-MOSFETs Exceeding Si Universality, C.H. Lee, T. Nishimura* N. Saido, K. Nagashio*, K. Kita*, A. Toriumi*, The University of Tokyo, *also with JST-CREST

We demonstrate for the first time very high electron mobility in Ge n-MOSFETs which exceeds the universal curve in Si-MOSFETs. This has been achieved by taking care of Ge/GeO_2 channel interface. Though the mobility is still limited by extrinsic scattering mechanisms, the results promise us to expect high performance Ge CMOS beyond Si CMOS.

3:10 p.m.

19.3 Germanium for Advanced CMOS Anno 2009: A SWOT Analysis (Invited), M. Caymax, G. Eneman, F. Bellenger, C. Merckling, A. Delabie, G. Wang, R. Loo, E. Simoen, J. Mitard, B. De Jaeger, G. Hellings, K. De Meyer, M. Meuris, M. Heyns, IMEC, also K.U. Leuven, FWO-Vlaanderen, MTM, IWT-Vlaanderen

Germanium has emerged as an important contender to take over as channel material from Si in high-performance logic applications for sub-22nm CMOS. This paper reviews the strengths and weaknesses of Germanium as material for MOSFETs, and reflects about opportunities (also outside CMOS) and treats (for its future use inside CMOS).

3:35 p.m.

19.4 Correlation Between Low-Field Mobility and High-Field Carrier Velocity in Quasi-Ballistic-Transport MISFETs Scaled Down to L_g=30nm, K. Tatsumura, M. Goto, S. Kawanaka, A. Kinoshita, Toshiba Corporation

The Lg dependence of velocity-mobility relationship is systematically investigated by using MISFETs with SiO_2, SiON, and various high-k. In the quasi-ballistic transport regime of Lg<50nm, mobility and scaling in Lg still play an important role on Ion improvement with velocity enhancement. High-k MISFETs do not show any particular velocity degradation in the high-energy transport. Our quantitative prediction reveals that aggressive Tinv scaling with novel higher-k dielectric should have a priority in order to reach the coming end of the roadmap.

4:00 p.m.

19.5 Understanding of Strain Effects on High-Field Carrier Velocity in (100) and (110) CMOSFETs under Quasi-Ballistic Transport, M. Saitoh, N. Yasutake, Y. Nakabayashi, K. Uchida*, T. Numata, Toshiba Corporation, *Tokyo Institute of Technology

We present the systematic study of strain effects on high-field carrier transport. Saturation drain current increase by strain in short-channel devices is strongly affected by the modulation of saturation velocity. It was found that the superiority of (110) CMOS to (100) CMOS is maintained at highly-strained conditions.

4:25 p.m

19.6 Physical Understandings of Si (110) Hole Mobility in Ultra-Thin Body pFETs by <110> and <111> Uniaxial Compressive Strain, K. Shimizu, T. Saraya, T. Hiramoto, University of Tokyo

The effects of (110) ultra-thin body pFETs on <111> and <110> uniaxial compressive strain have been investigated systematically for the first time. It is found that the strain effect in <110> UTB pFET severely degraded due to small change in conduction effective mass. It is also confirmed by measurements and band calculation that <111> UTB pFET is free from this degradation mechanisms and achieves larger hole mobility enhancement than <110> UTB pFET, caused by larger effective mass change and smaller density-of-state reduction.

4:50 p.m.
19.7 Direct Observation of Subband Structures in (110) pMOSFETs under High Magnetic Field: Impact of Energy Split Between Bands and Effective Masses on Hole Mobility, T. Takahashi, G. Yamahata, J. Ogi, T. Kodera, S. Oda, K. Uchida*, Tokyo Institute of Technology, *also with PRESTO

The band structures and carrier transport in (110) pFETs are thoroughly studied over a wide temperature range under high magnetic fields, for the first time. The energy difference between lower energy and higher energy bands is estimated. The effective mass of each band is directly obtained from the SdH analysis. Because of the worse mobiliy in higher energy band, mobility enhancement of (110) pFETs will be possible if we can further enhance the energy split between bands.

Session 20: Quantum, Power and Compound Semiconductors – III-V HEMT Device Scaling

Tuesday, December 8, 2:15 p.m.
Key Ballrooms 3 and 4
Co-Chairs: *Berinder Brar, Teledyne Scientific and Imaging*
Hong Wang, Nanyang Technological University

2:15 p.m.
Introduction

2:20 p.m.
20.1 30 nm $In_{0.7}Ga_{0.3}As$ Inverted-Type HEMTs with Reduced Gate Leakage Current for Logic Applications, T.-W. Kim, D.-H. Kim, J.A. del Alamo, Massachusetts Institute of Technology

We have fabricated and demonstrated 30 nm $In_{0.7}Ga_{0.3}As$ Inverted HEMTs with outstanding logic performance, scalability and high frequency characteristics. This work suggest that III-V FET designs similar to the inverted HEMT but with a high-K gate dielectric have potential for scaling to very small dimensions for future logic applications.

2:45 p.m.

20.2 Logic Performance Evaluation and Transport Physics of Schottky-Gate III-V Compound Semiconductor Quantum Well Field Effect Transistors for Power Supply Voltages (V_{CC}) Ranging from 0.5V to 1.0V, G. Dewey, R. Kotlyar, R. Pillarisetty, M. Radosavljeric, T. Rakshit, H. Then, R. Chau, Intel Corporation

The logic performance of Schottky-gate $In_{0.7}Ga_{0.3}As$ QWFETs is measured and evaluated against that of advanced Strained Si MOSFETs from Vcc = 0.5 to 1.0V at constant I_{off}. Effective carrier velocity measurements and temperature dependent studies are used to understand the device performance and transport physics for the same voltage range.

3:10 p.m.

20.3 Performance Analysis of Ultra-Scaled InAs HEMTs, N. Kharche, G. Klimeck, D.-H. Kim*, J.A. del Alamo**, M. Luisier, Purdue University, *Teledyne Scientific & Imaging LLC, **Massachusetts Institute of Technology

III-V High Electron Mobility Transistors (HEMTs) have emerged as potential candidates for high-speed, low-power logic applications beyond Si-CMOS technology. Device simulation may help experimentalists scale the gate length of HEMTs below 30nm to keep following Moore's law. However, performance predictions of not-yet-fabricated transistors require a simulator that reproduces available experimental data. We demonstrate very good quantitative agreement of our simulations with experimental data on InAs HEMTs with gate lengths ranging from 30 to 50nm.We explore the performance of 20 nm gate length InAs HEMTs and show that such devices are perfectly viable with slight fabrication modifications.

3:35 p.m.
20.4 Quantum Capacitance in Scaled Down III-V FETs, D. Jin, D. Kim, Taewoo Kim, J.A. del Alamo, Massachusetts Institute of Technology

We developed a model for gate capacitance including quantum capacitance in III-V FETs. The model agrees with experiments on scaled InGaAs and InAs FETs. Our model suggests that quantum capacitance dominates in scaled devices and that strain engineering and quantization are required to increase the effective mass in future scaled devices.

4:00 p.m.
20.5 N-polar GaN-based Highly Scaled Self-aligned MIS-HEMTs With State-of-the-art $f_T.L_G$ Product of 16.8 GHz-µm (Late News), Nidhi, S. Dasgupta, D.F. Brown, S. Keller, J.S. Speck and U.K. Mishra, University of California Santa Barbara

In this paper, we describe a gate-first self-aligned MBE InGaN regrowth methodology for fabricating N-polar GaN-based MIS-HEMTs which exhibit ultra-low contact resistances of 23 Ω-µm, which is comparable to the lower band-gap technologies. These devices, not only show state-of the-art $f_T.L_G$ product values of 16.8 GHz- µm for 130 nm gate length for GaN, but also show exceptional performance at low supply voltages (VDS = 500 mV), thereby making GaN competitive not only to wide band-gap materials like SiC but also to low band-gap technologies by InGaAs HEMTs and InSb by having low knee voltages, high drive currents while still demonstrating relatively large breakdown voltages for unipolar (non-CMOS like) operation.

Session 21: Modeling and Simulation – CMOS Process and Optimization
Tuesday, December 8, 2:15 p.m.
Key Ballroom 6
Co-Chairs: *Pierpaolo Palestri, University of Udine*
Taiji Noda, Panasonic Corp.

2:15 p.m.
Introduction

2:20 p.m.
21.1 A Voltage Scaling Model for Performance Evaluation in Digital CMOS Circuits, K. von Arnim, K. Schruefer, T. Baumann, K. Hofmann, T. Schulz, C. Pacha, J. Berthold, Infineon Technologies

We present an easy to use method to extrapolate digital circuit perform-ance and power from nominal to worst-case operating conditions. It al-lows the circuit designer to explore the design space continuously over voltages, temperatures and process conditions. Voltage scaling is identified as a key challenge for the 22nm technology node.

2:45 p.m.
21.2 Benchmarking the Device Performance at Sub 22nm Node Technologies using an SoC Framework, M. Shrivastava, B. Verma, M.S. Baghini, C. Russ*, D.K. Sharma, H. Gossner*, V.R. Rao, Indian Institute of Technology-Bombay, *Infineon Technologies

We predicted the System-on-Chip (SoC) performance of various planar and non-planar SOI devices. Non-planar devices perform poorly in comparison to Ultra thin body (UTB) planar SOI MOSFET and are not the ideal choice for SoC applications. New strategies towards device optimization are demonstrated, which further improves SoC performance of UTB-MOSFET.

3:10 p.m.
21.3 Nonlinear Dynamics Approach in Modeling of the On-State-Spreading - Related Voltage and Current Transients in 90nm CMOS Silicon Controlled Rectifiers, D. Pogany, D. Johnsson*, S. Bychikhin, K. Esmark*, P. Rodin**, E. Gornik, M. Stecher*, H. Gossner*, Vienna University of Technology, *Infineon Technologies, **Ioffe Physicotechnical Institute

Using a theory of nonlinear dynamical systems we model the on-state spreading related voltage, current and on-state width transients in 90nm CMOS silicon controlled rectifiers. The model explains well voltage transients during the rising edge of ESD pulses and predicts a non-trivial dependence of device voltage on number of triggering regions.

3:35 p.m.
21.4 Atomistic Process Modeling Based on Kinetic Monte Carlo and Molecular Dynamics for Optimization of Advanced Devices (Invited), L. Pelaz, L.A. Marques, M. Aboy, P. Lopez, I. Santos, R. Duffy*, University of Valladolid, *Tyndall National Institute

Combined Molecular Dynamics and Kinetic Monte Carlo simulations are used to gain physical understanding and enable process optimization in advanced devices. Minimization of defects beyond the amorphous/crystalline interface advocates lowering dynamic annealing during implant. Thermal budget for the removal of defects in advanced millisecond anneals is evaluated. Alternatives to overcome the imperfect regrowth of narrow Si structures are proposed. The compromise between implant and anneal parameters for doping of FinFETs are presented, considering lateral diffusion and activation.

4:00 p.m.
21.5 Modeling of Stress-Retarded Orientation-Dependent Oxidation: Shape Engineering of Silicon Nanowire Channels, F.-J. Ma, S.C. Rustagi, H. Zhao, G.S. Samudra*, N. Singh, K.D. Budhaaraju, G.Q. Lo, D.L. Kwong, Astar Institute of Microelectronics, *National University of Singapore

The stress dependent oxidation of silicon fins has been characterized and modeled. The experimental characterization reveals that the shape of the initial fins strongly influence the evolution of nanowire channel shapes. A significant retardation of oxide growth rate is observed even high temperature of 975C. The orientation dependent thin-oxide regime and visco-elastic models are improved to explain the experimental results.

4:25 p.m.
21.6 Compact AC Modeling and Analysis of Cu, W, and CNT Based Through-Silicon Vias (TSVs) in 3-D ICs, C. Xu, H. Li, R. Suaya*, K. Banerjee, University of California, Santa Barbara, *Mentor Graphics Corporation

This is the first accurate compact CGRL model for TSVs with consideration of MOS effect, AC conduction, skin effect and eddy current. The model can also be applied to TSVs with CNT bundles. MWCNT TSVs can offer smaller or comparable high-frequency resistance, but cannot offer a non-negligible delay reduction.

Session 22: Displays, Sensors and MEMS – Heterogeneous Integration for Energy Harvesting and Photonics
Tuesday, December 8, 2:15 p.m.
Key Ballroom 5
Co-Chairs: Christopher Hierold, ETH Zurich
Karl Bohringer, University of Washington

2:15 p.m.
Introduction

2:20 p.m.
22.1 Smart Scalable Systems: A Bottom-up Approach of Building Complex Systems (Invited), S. Kwon, Seoul National University

Manufacturing of highly heterogeneous and complex system has been achieved through self-assembly of large number of heterogeneous components. Optofluidic generation and microfluidic self-assembly of various microparts are reviewed under theme of smart scalable systems, a bottom-up approach of building complex systems.

2:45 p.m.
22.2 3D Heterogeneous Opto-Electronic Integration Technology for System-on-Silicon (SOS), K.-W. Lee, A. Noriki, K. Kiyoyama, S. Kanno, R. Kobayashi, W.-C. Jeong, J.-C. Bea, T. Fukushima, T. Tanaka, M. Koyanagi, Tohoku University

We developed novel heterogeneous integration technology of LSI, MEMS and optoelectronic devices by implementing 3D heterogeneous opto-electronic multi-chip module for realizing 3D opto-electronic integrated system-on-silicon (SOS). The electrical interposer mounted with LSI and MEMS chips and the optical interposer embedded with VCSEL and PD chips are precisely bonded. Opto-electronic devices are electrically connected TSVs which were formed into the interposers. Micro-fluidic channels are formed into the interposer by wafer direct bonding. 3D heterogeneous opto-electronic multi-chip module is successfully implemented for the first time.

3:10 p.m.
22.3 Anomalous Stress Effects in Ultra-Thin Silicon Chips on Foil, M.-U. Hassan, H. Rempp, T. Hoang, H. Richter, N. Wacker, J.N. Burghartz, Institute for Microelectronics Stuttgart

CMOS transistors, resistors and current mirrors on 20µm thin, flexible chips for system-in-foil (SiF) applications exhibit an apparently anomalous and transient piezoresistive effect. This effect results from a transformation from uniaxial to biaxial stress according to the Poisson ratio of the epoxy glue used for chip attachment.

3:35 p.m.
22.4 Microfabricated Radioisotope-powered Active RFID Transponder, S. Tin, A. Lal, Cornell University

We demonstrate a microfabricated Ni-63 radioisotope-powered RFID transponder realized with a SAW device as the transmission frequency selector. With MEMS microfabrication and vacuum packaging, the integrated RFID/ sensor system powered with 100 year halflife Ni-63 source can work autonomously for decades, which can revolutionize long term reliable sensing and monitoring.

4:00 p.m.
22.5 First Autonomous Wireless Sensor Node Powered by a Vacuum-Packaged Piezoelectric MEMS Energy Harvester, R. Elfrink, V. Pop, D. Hohlfeld, T.M. Kamel, S. Matova, C. de Nooijer, M. Jambunathan, M. Goedbloed, L. Caballero, M. Renaud, J. Penders, R. van Schaijk, IMEC

This work shows the results of aluminum nitride based MEMS energy harvesters. The used vacuum package is essential for reliability and preventing air damping. The average power consumption of a prototype wireless autonomous sensor system is less then 10 μW and has been fully delivered by a vibration energy harvester.

4:25 p.m.
22.6 Surface Nanostructure Optimization for Solar Energy Harvesting in Si Thin Film Based Solar Cells, J.S. Li, H.Y. Yu*, S.M. Wong*, G. Zhang, G.-Q. Lo, D.-L. Kwong, Institute of Microelectronics, *also Nanyang Technological University

The solar energy harvesting of Si thin films with Si nanocone or nanopillar array decorated surfaces are systematically studied by simulation for the first time. It is found that the high and broad-width light absorption around 2.5 eV is the key to achieve high efficiencies for both nanostructures. Nanostructure dimensions are optimized based on the enhanced light scattering, and thus the prolongated optical path around this energy. This work provides a practical guideline to design and fabricate Si thin film solar cells with high efficiency matching the bulk Si record.

4:50 p.m.
22.7 A Novel Photovoltaic Nanodevice Based on the Co-Integration of Silicon Micro and Nanowires Prepared by Electroless Etching with Conformal Plasma Doping, H.-D. Um, J.-Y. Jung* X. Li, S.-W. Jee, K.-T. Park, H.-S. Seo, S.A. Moiz, S.-W. Lee*, J.-Y. Ji*, C.T. Kim*, M.S. Hyun**, Y.C. Park**, J.M. Yang**, J.-H. Lee, Hanyang University, *ADP engineering CO., **National Nanofab Center

Periodically patterned co-integration of silicon microwires (MWs) and nanowires (NWs) were applied for a novel photovoltaic (PV) nanodevice. Si MWs that form a radial p-n junction were located in between the dense array of Si NWs. These wire arrays were cost-effectively defined by metal-assisted electroless wet etching. Highest values of short circuit current and CE at 1.5AM illumination were recorded as 24.89 mA/cm^2 and 8.45%.

5:15 p.m.
22.8 0.9µm Pitch Pixel CMOS Image Sensor Design Methodology, K. Itonaga, K. Mizuta, T. Kataoka, M. Yanagita, S. Yamauchi, H. Ikeda, T. Haruta, S. Matsumoto, M. Harasawa, T. Matsuda, A. Matsumoto, I. Mizuno, T. Kameshima, I. Sugiura, T. Umebayashi, K. Ohno, T. Hirayama, Sony Corporation

We proposed the constant-light-diffraction-scaling methodology in order to design the CMOS image sensor(CIS). We developed a high performance guideline, and verified it using CISs with various pixel pitches and number of metal wiring layers. Using this guideline, we realized the first ever successful fabrication of 1.12 and 0.9µm pitch CISs.

Session 23: Solid State and Nanoelectronic Devices – Silicon Photonics, Carbon Devices and Integration
Tuesday, December 8, 2:15 p.m.
Key Ballrooms 1 and 2
Co-Chairs: Zhihong Chen, IBM TJ Watson Research Center
Max Lemme, Harvard University

2:15 p.m.
Introduction

2:20 p.m.
23.1 Can Carbon Nanotube Transistors be Scaled Without Performance Degradation?, A.D. Franklin, G. Tulevski, J.B. Hannon, Z. Chen, IBM TJ Watson Research Center

Investigation of effects of channel length scaling on carbon nanotube transistors by varying device lengths on the same nanotube. Results show that scaling improves performance: substantial increases in on-current, resistances closer to the quantum limit than have ever been reported, and the shortest (~30 nm) well-behaving devices to date.

2:45 p.m.
23.2 Metal/Graphene Contact as a Performance Killer of Ultra-high Mobility Graphene - Analysis of Intrinsic Mobility and Contact Resistance -, K. Nagashio, T. Nishimura, K. Kita, A. Toriumi, The University of Tokyo

The contact resistance (RC) between graphene and metal electrodes is crucially important for achieving potentially high performance of graphene from both physics and practical viewpoints. This paper discusses the metal/graphene contact properties by separating from the intrinsic conduction of graphene.

3:10 p.m.

23.3 Silicon Photonics Technologies for Monolithic Electronic-Photonic Integrated Circuit (EPIC) Applications: Current Progress and Future Outlook (Invited), K.-W. Ang, T.-Y. Liow, Q. Fang, M.B. Yu, F.F. Ren, J. Zhang, J.W. Ng, J.F. Song, Y.Z. Xiong, G.Q. Lo, D.-L. Kwong, Institute of Microelectronics

This paper reviews the current status of the EPIC development, and provides Outlook for the Monolithic Integration of Si Micro- and Nani-Photonics and its Potential Applications in Near Future.

3:35 p.m.

23.4 VMR: VLSI-Compatible Metallic Carbon Nanotube Removal for Imperfection-Immune Cascaded Multi-Stage Digital Logic Circuits using Carbon Nanotube FETs, N. Patil, A. Lin, J. Zhang, H. Wei, K. Anderson, H.-S.P. Wong, S. Mitra, Stanford University

Metallic Carbon Nanotubes (CNTs) pose a major barrier for VLSI Carbon Nanotube Field Effect Transistor (CNFET) technology. We demonstrate VLSI-compatible Metallic CNT Removal (VMR) using electrical breakdown of metallic CNTs. We demonstrate cascaded logic circuits (inverter, NAND, multiplexer, XNOR). VMR overcomes the limitations of existing metallic CNT removal techniques.

4:00 p.m.

23.5 Monolithic Three-Dimensional Integrated Circuits using Carbon Nanotube FETs and Interconnects, H. Wei, N. Patil, A. Lin, H.-S.P. Wong, S. Mitra, Stanford University

Three Dimensional (3D) integration circuits stacking is a superior circuit design technique which can boost functional density & performance, reduce design size and power consumption. Carbon Nanotubes Field Effect Transistors (CNFET) are regarded as promising candidates as extensions to silicon CMOS due to excellent intrinsic delay at the device level. For the first time, we experimentally demonstrate a VLSI-compatible monolithic 3D ICs consisting of CNFETs and CNT interconnect integrated over 3 levels using standard vias for inter-level connection.

4:25 p.m.

23.6 High-Speed Graphene Interconnects Mono-lithically Integrated with CMOS Ring Oscillators Operating at 1.3GHz, X. Chen, K.-J. Lee*, D. Akinwande, G.F. Close, S. Yasuda**, B. Paul^, S. Fujita**, J. Kong*, H.-S.P. Wong, Stanford University, *Massachusetts Institute of Technology, **Toshiba Corporation, ^Toshiba America Research

We present the first experimental demonstration of graphene interconnects monolithically integrated with CMOS low-swing ring oscillator circuit, operating at 1.3 GHz. Large area graphene is synthesized using a VLSI-compatible CVD synthesis method. The graphene is integrated with CMOS circuits to serve as interconnects for ring oscillators.

Session 24 – 2009 IEDM Evening Panel Discussion
Tuesday, December 8, 8:00 p.m.
Holiday Ballroom 4-6

"Managing Innovation: An Oxymoron?"

Organizers: Jeff Welser, IBM
Rakesh Kumar, TCX, Inc.
In cooperation with the IEEE Technology Management Council

While balancing innovation and delivering new products has always been a challenge for the semiconductor industry, the current state of affairs is requiring a major re-examination of these challenges. Although it is commonly believed that technical challenges for shrinking geometries can be overcome, managing new technology innovation under shrinking budgets is a huge challenge in the present environment. The size of internal research organizations is shrinking, and there is pressure to use external organizations for cooperative research. On the product side, demands for reduced time-to-market make it more challenging to get new research ideas implemented into production. So, how are we to get new research ideas into products in a timely manner?

The rapid emergence of the fabless and asset-lite business models, as well as increased reliance on R&D alliances and collaborative work with universities, adds more complexity to the entire research/product development landscape.

The objectives of this panel are to provide a perspective on the following:

1. Real life examples of how they schedule innovations of either external or internal research into fruition in timely product deliveries
2. The impact of managing these innovation challenges on career development, especially for young professionals.

The panel will explore some key questions such as:

- How are new research ideas developed and supported within your company?
- How do you utilize external research or alliances to bring innovation to your product line?
- How do foundries and the customers work together to create unique value?
- Given the changing model of innovation in the industry, what's different about R&D career paths of young engineers in the field today versus in the 1980's and the 1990's? What should they be doing to enhance their careers in the 2010's?
- Who will be writing IEDM papers in 10 years? Will the authors get recognition and support within their organizations for invention disclosures and paper publication/presentations?

Moderator: Rakesh Kumar, TCX, Inc.

Panelists:
Jim Clifford, Qualcomm
Bijan Davari, IBM
Gilbert Declerck, IMEC
Paolo Gargini, Intel
Lisa Su, Freescale
Jack Sun, TSMC
Hisatsune Watanabe, SELETE

Session 25: IEDM Evening Panel Discussion
Holiday Balllroom 1-3
Tuesday, December 8, 8:00 p.m.

"When and How Will the High Mobility Substrates Impact the Si Technology Roadmap?"

Organizer: Dimitri Antoniadis, MIT

The classical MOSFET scaling era has been over approximately since the 130 nm CMOS technology. While the cadence of geometric scaling has continued, new process elements (strain) and new materials (hi-K/metal gate) had to be introduced in order to provide improved transistor performance with scaling. In particular, strain has been very effective in increasing key carrier transport parameters, "thermal velocity" and mobility in and has resulted in significant improvement of nFETs and dramatic improvement of pFETs. But strained-Si is reaching its physical limits and alternative approaches are being sought to further enhance carrier transport properties via the introduction of "high-mobility" materials on Si. At this point, SiGe and Ge appear to be suitable candidates primarily for hole channels while various III-V materials are being investigated primarily for electron channels.
The objective of this panel is to provide a perspective on the following:

1. What is a possible or likely scenario for the introduction of new channel materials in the 15 nm CMOS node? Is it possible with the currently anticipated geometric scaling cadence of gate-contacted pitch?

2. What are the key milestones that must be demonstrated before industry would invest heavily in developing this technology?

3. Is it possible that suppliers would be able to provide the necessary equipment for this materials integration? – Would need a supplier rep on the panel for this?

4. What are the likely show-stoppers for the introduction of this technology element?

Panelists:
Robert Chau, Intel
Gene Fitzgerald, MIT
Krishna Saraswat, Stanford University
Ghavam Shahidi, IBM
Thomas Skotnicki, STMicroelectronics
Shinichi Takagi, University of Tokyo
Yee-Chia Yeo, Nat'l Univ. of Singapore

Session 26: Displays, Sensors and MEMS – Medical and Bioelectronics
Wednesday, December 9, 9:00 a.m.
Holiday Ballroom 6
Co-Chairs: *Chris van Hoof, Holst Centre*
Kwang-Seok Yun, Sognag University

9:00 a.m.
Introduction

9:05 a.m.
26.1 Implantable Wireless Dosimeters for Radiation Oncology (Invited), T. Maleki, C. Son, B. Ziaie, Purdue University,

In this abstract, we will discuss two radiation detectors developed in our lab to remotely monitor the radiation dose received by a tumor. The first one is a MEMS-based miniature ionization-chamber and the second transducer is based on a highly sensitive solid-state structure.

9:30 a.m.
26.2 A Curvable Silicon Retinal Implant, R. Dinyari, J.D. Loudin, P. Huie, D. Palanker, P. Peumans, Stanford University

We have developed a curvable photovoltaic monolithic retinal implant that requires no electrical power or data connection. The implant consists of a two-dimensional network of miniature silicon solar cells that directly stimulate the retina. A MEMS process isolates adjacent pixels and makes the arrays curvable.

9:55 a.m.

26.3 Novel T-Channel Nanowire FET with Built-in Signal Amplification for pH Sensing, K.-S. Shin, K. Lee*, J.Y. Kang*, C.O. Chui, University of California, Los Angeles, *Korea Institute of Science and Technology

We have proposed a novel T-shape channel nanowire FET with a built-in signal amplification mechanism. Relying on a similar operating principle to that of the bipolar transistor, a significant improvement of 20-50x in pH detection sensitivity has been experimentally demonstrated over the co-fabricated, conventional nanowire FET sensor.

10:20 a.m.

26.4 A Novel Flash-Ion-Sensitive Field-Effect Transistor (FISFET) with HfO_2/Gd_2O_3(Gd) Nano-crystal/SiO_2 Sensing Membranes under Super Nernstian Phenomenon for pH and Urea Detection, T.-F. Lu, J.-C. Wang, C.-S. Lai, C.-M. Yang, M.-H. Wu, C.-P. Liu*, R.-S. Huang*, Y.-C. Fang**, Chang Gung University, *National Cheng-Kung University, **Chung-Shan Institute of Science and Technology

A novel Flash-Ion-Sensitive Field-Effect Transistor (FISFET) with Gd_2O_3 nanocrystal was proposed to obtain super Nernstian properties by charge trapping effect on pH detection.The sensing properties including high pH response (~80 mV/pH) and low urea concentration detection (1-10 mM) based on FISFET device were obtained.

10:45 a.m.
26.5 Highly Sensitive and Selective Label-Free Detection of Cardiac Biomarkers in Blood Serum with Silicon Nanowire Biosensors, G.-J. Zhang, Z.H.H. Luo, M.J. Huang, G.K.I. Tay, E.-J.A. Lim, Y. Chen, Institute of Microelectronics

Arrays of highly ordered silicon nanowire (SiNW) are fabricated using complementary metal-oxide semiconductor (CMOS) field effect transistor-compatible technology, and the ultrasensitive, label-free, electrical detection of cardiac biomarker in blood serum using the array sensor is demonstrated. The SiNW array biosensor allows for real-time detection of cardiac biomarker in desalted serum, more importantly, multiplexed detection of cardiac biomarkers in untreated and non-desalted blood serum.

11:10 a.m.
26.6 A Novel Model for (percolating) Nanonet Chemical Sensors for Microarray-based E-Nose Applications,
J. Go, V.V. Sysoev*, A. Kolmakov**, N. Pimparkar, M.A. Alam, Purdue University, *Saratov State Technical University, **Southern Illinois University

Our numerical simulations for percolating multi-nanowire (NW) chemical sensors demonstrate the fundamental role of potential barriers at NW-to-NW junctions in dictating sensor response and how the sensor response changes with NW density. Based on this model, we also explain the enhancement of detection limit at a high-density NW network sensor.

Session 27: Memory Technology – 3D Memory: Non-volatile Memory Architectures
Wednesday, December 9, 9:00 a.m.
Key Ballrooms 7, 9 and 10
Co-Chairs: Agostino Pirovano, Numonyx
Klaus Schuegraf, Applied Materials

9:00 a.m.
Introduction

9:05 a.m.
27.1 A Stackable Cross Point Phase Change Memory, D.C. Kau, S. Tang*, I.V. Karpov, R. Dodge*, B. Klehn, J.A. Kalb, J. Strand*, A. Diaz*, N. Leung, J. Wu*, S. Lee, T. Langtry*, K.-W. Chang, C. Papagianni*, J. Lee, J. Hirst*, S. Erra, E. Flores*, N. Righos, H. Castro*, G. Spadini, Intel Corp., *Numonyx B.V.

A phase change memory cell is built by coupling PCM with OTS (PCMS) and integrated in a true cross point array. Multiple layers of PCMS arrays can be stacked over CMOS circuits. This fast, durable, and dense memory for random access and storage applications provides a promising, scalable NVM technology.

9:30 a.m.
27.2 Monolithic Integration of NEMS-CMOS with a Fin-flop Actuated Channel Transitor (FinFACT), J.-W. Han, J.-H. Ahn, M.-W. Kim, J.-B. Yoon, Y.-K. Choi, KAIST

Independent-gate FinFET and mechanically flip-flopped fin NEMS memory is co-fabricated with CMOS process. The proposed NEMS memory is featured by the laterally actuated channels with various widths and a 10nm air-gap thickness, which provides a sensing current window of 10^7, data retention time over 10^4 sec, and endurance over 10^3 cycles in air.

9:55 a.m.
27.3 Optimal Device Structure for Pipe-shaped BiCS Flash Memory for Ultra High Density Storage Device with Excellent Performance and Reliability, M. Ishiduki, Y. Fukuzumi, R. Katsumata, M. Kito, M. Kido, H. Tanaka, Y. Komori, Y. Nagata*, T. Fujiwara, T. Maeda, Y. Mikajiri, S. Oota, M. Honda, Y. Iwata, R. Kirisawa, H. Aochi, A. Nitayama, Toshiba Corporation, *Toshiba Information Systems Corporation

An asymmetric source/drain profile for select gate and metal salicided control gate are successfully realized on Pipe-shaped Bit Cost Scalable (P-BiCS) Flash memory to achieve data storage device with excellent performance and reliability.

10:20 a.m.
27.4 Study of Sub-30nm Thin Film Transistor (TFT) Charge-Trapping (CT) Devices for 3D NAND Flash Application, T.-H. Hsu, H.-T. Lue, C.-C. Hsieh, E.-K. Lai, C.-P. Lu, S.-P. Hong, M.-T. Wu, F.H. Hsu, N.Z. Lien, J.-Y. Hsieh, L.-W. Yang, T. Yang, K.-C. Chen, K.-Y. Hsieh, R. Liu, C.-Y. Lu, Macronix International Co. Ltd.

Sub-30nm TFT CT NAND flash devices have been extensively studied. Our results show that as TFT devices scale down to sub-30nm, the DC characteristics approach those of the bulk devices. However, grain boundaries only affects the DC characteristics but does not impact the memory window. A sub-30 nm TFT BE-SONOS NAND device with MLC capability and good retention is demonstrated.

10:45 a.m.
27.5 One-Transistor Nonvolatile SRAM (ONSRAM) on Silicon Nanowire SONOS, S.-W. Ryu, J.-W. Han, D.-I. Moon, Y.-K. Choi, KAIST

We have developed One-transistor Nonvolatile SRAM (ONSRAM) on a silicon nanowire (SiNW) SONOS. The nonvolatile memory (NVM) property was constructed by employing O/N/O gate dielectric stacks as an electron storage node, and SRAM operation is stemmed from latch phenomena of a floating body in SiNW. An abrupt inverter switching, superior sensing current (>23μA), and high interference immunity between SRAM and NVM approve the feasibility for the scheme of ONSRAM.

11:10 a.m.
27.6 A Stacked SONOS Technology, Up to 4 Levels and 6nm Crystalline Nanowires, with Gate-All-Around or Independent Gates (ΦFlash), Suitable for Full 3D Integration, A. Hubert, E. Nowak, K. Tachi, V. Maffini-Alvaro, C. Vizioz, C. Arvet**, J.-P. Colonna, J.-M. Hartmann, V. Loup, L. Baud, S. Pauliac, V. Delaye, C. Carabasse, G. Molas, G. Ghibaudo*, B. De Salvo, O. Faynot, T. Ernst, CEA-LETI MINATEC, *IMEP-LAHC INPG MINATEC, **STMicroelectronics

We present the first experimental study of 3D SONOS memory with 4-level crystalline stacked nanowire channels. Results with 6nm nanowires show high programming windows with excellent retention. The technology is also integrated in independent double gate memory (ΦFlash). The process to fully disconnect the levels for 3D integration is discussed.

11:35 a.m.
27.7 Future Directions of Non-Volatile Memory in Compute Applications (Invited), A. Fazio, Intel Corp.

NAND's new position in the compute memory hierarchy imposes new considerations for scaling to smaller lithography nodes and tightly links NAND with the external controller. Likewise, widespread acceptance of future NVM in the compute memory hierarchy will be determined by ability to meet both cost and performance criteria.

Session 28: CMOS Devices and Technology – Advanced High-K Metal Gate SoC and High Performance CMOS Platforms
Wednesday, December 9, 9:00 a.m.
Key Ballrooms 8, 11 and 12
Co-Chairs: *Geoffrey Yeap, Qualcomm Inc.*
Klaus Schruefer, Infineon Technologies

9:00 a.m.
Introduction

9:05 a.m.
28.1 A 32nm SoC Platform Technology with 2nd Generation High-k/Metal Gate Transistors Optimized for Ultra Low Power, High Performance, and High Density Product Applications, C.-H. Jan, M. Agostinelli, M. Buehler, Z.-P. Chen, S.-J. Choi, G. Curello, H. Deshpande, S. Gannavaram, W. Hafez, U. Jalan, M. Kang, P. Kolar, K. Komeyli, B. Landau, A. Lake, N. Lazo, S.-H. Lee, T. Leo, J. Lin, N. Lindert, S. Ma, L. McGill, C. Meining, A. Paliwal, J. Park, K. Phoa, I. Post, N. Pradhan, M. Prince, A. Rahman, J. Rizk, L. Rockford, G. Sacks, A. Schmitz, H. Tashiro, C. Tsai, P. Vandervoorn, J. Xu, L. Yang, J.-Y. Yeh, J. Yip, I. Young, K. Zhang, Y. Zhang, P. Bai, Intel Corporation

A leading edge 32nm high-k/metal gate transistor technology has been optimized for SoC platform applications that span a wide range of power, performance, and feature space. This technology has been developed to be modular, offering mix-and-match triple transistors, interconnects, RF/analog passive elements, embedded memory, and noise mitigation options.

9:30 a.m.

28.2 Competitive and Cost Effective High-k based 28nm CMOS Technology for Low Power Applications, F. Arnaud[1], A.Thean[2], M. Eller[3], M. Lipinski[3], Y.W. Teh[4], M. Ostermayr[3], K. Kang[6], N.S. Kim[4], K. Ohuchi[7], J-P. Han[3], D.R. Nair[2], J. Lian[3], S. Uchimura[7], S. Kohler[1], S. Miyaki[8], P. Ferreira[1], J.-H. Park, M. Hamaguchi, K. Miyashita, R. Augur[5], Q. Zhang[2], K. Strahrenberg, S. ElGhouli[1], J. Bonnouvrier[1], F. Matsuoka[7], R. Lindsay[3], J. Sudijono[4], F.S. Johnson[5], J.H. Ku[6], M. Sekine[8], A. Steegen[2], R. Sampson[1], IBM SRDC, [1]STMicroelectronics, [2]IBM Microelectronics, [3]Infineon Technologies, [4]Chartered Semiconductor Manufacturing, [5]GlobalFoundries, [6]Samsung Electronics, [7]Toshiba, [8]NEC-EL

We present a cost-effective 28nm CMOS technology for low power applications based on a high-k. We report raw gate densities up to 4200 kGate/mm^2. Our SRAM bit-cell (0.120mm^2) has a demonstrated SNM of 213mV at 1V. I_{on} are increased +35% & +10%, for nFET and pFET versus poly/SiON. Leading edge AVT~2mV.um has been demonstrated. Optimized interconnection based lowk~2.4 allows high density with competitive R-C.

9:55 a.m.

28.3 A Novel "Hybrid" High-k/Metal Gate Process For 28nm High Performance CMOSFETs, C.M. Lai, C.T. Lin, L.W. Cheng, C.H. Hsu, J.T. Tseng, T.F. Chiang, C.H. Chou, Y.W. Chen, C.H. Yu, S.H. Hsu, C.G. Chen, Z.C. Lee, J.F Lin, C.L. Yang, G.H. Ma, S.C. Chien, United Microelectronics Corporation

A "hybrid" HK/MG integration scheme is proposed in this paper to accomplish high performance 28nm CMOSFETs by integrating gate first/last techniques for N/PFET respectively. A remarkable NFET mobility (95% of n^+poly/SiON@1MV/cm) and low VTH (0.25 V) were achieved through optimized processes. For PFET, extra 30% performance improvement was achieved by GL because of strain boost and VFB roll off elimination.

10:20 a.m.

28.4 High Performance 32nm Logic Technology Featuring 2nd Generation High-k + Metal Gate Transistors, P. Packan, S. Akbar, M. Armstrong, D. Bergstrom, M. Brazier, H. Deshpande, K. Dev, G. Ding, T. Ghani, O. Golonzka, W. Han, J. He, R. Heussner, R. James, J. Jopling, C. Kenyon, S-H. Lee, M. Liu, S. Lodha, B. Mattis, A. Murthy, L. Neiberg, J. Neirynck, S. Pae, C. Parker, L. Pipes, J. Sebastian, J. Seiple, B. Sell, A. Sharma, S. Sivakumar, B. Song, A. St. Amour, K. Tone, T. Troeger, C. Weber, K. Zhang, Y. Luo, S. Natarajan, Intel Corporation

A 32nm logic technology for high performance microprocessors is described. 2nd generation high-k + metal gate transistors provide record drive currents at the tightest gate pitch reported for any 32nm or 28nm logic technology. NMOS drive currents are 1.62mA/um Idsat and 0.231mA/um Idlin at 1.0V and 100nA/um Ioff. PMOS drive currents are 1.37mA/um Idsat and 0.240mA/um Idlin at 1.0V and 100nA/um Ioff. The impact of SRAM cell and array size on Vccmin is reported.

10:45 a.m.

28.5 Ultra Low-EOT (5 Å) Gate-First and Gate-Last High Performance CMOS Achieved by Gate-Electrode Optimization, L.-Å. Ragnarsson, Z. Li, J. Tseng, T. Schram, E. Rohr, M.J. Cho, T. Kauerauf, T. Conard, Y. Okuno, B. Parvais, P. Absil, S. Biesemans, T.Y. Hoffmann, IMEC

A novel gate-first approach is used to produce devices with EOT ~5Å and Tinv ~8Å. The n and pMOS Ion is 1.4 mA/µm and 0.6 mA/µm respectively at V_{DD}=1V and I_{off}=100 nA/µm. The technology further offers low V_T, good V_T-uniformity, and V_T-matching and high fT at ~290 GHz.

11:10 a.m.

28.6 Hybrid FDSOI/Bulk High-k/Metal Gate Platform for Low Power (LP) Multimedia Technology, C. Fenouillet-Beranger*, P. Perreau*, L. Pham-Nguyen, S. Denorme, F. Andrieu*, L. Tosti*, L. Brevard*, O. Weber*, S. Barnola*, T. Salvetat*, X. Garros*, M. Casse*, C. Leroux*, J.P. Noel*, O. Thomas*, B. Le-Gratiet, F. Baron, M. Gattefait, Y. Campidelli, F. Abbate, C. Perrot, C. de-Buttet*, R. Beneyton, L. Pinzelli, F. Leverd, P. Gouraud, M. Gros-Jean, A. Bajolet, C. Mezzomo, C. Leyris, S. Haendler, D. Noblet, R. Pantel, A. Margain, C. Borowiak, E. Josse, N. Planes, D. Delprat^, F. Boedt^, K. Bourdelle^, B.Y. Nguyen^**, F. Boeuf, O. Faynot*, T.Skotnicki, STMicroelectronics, *CEA-LETI MINATEC, **also IMEP, MINATEC, ^SOITEC

In this paper, we present FD-SOI with High-K and Single Metal gate as a possible candidate for LP multimedia technology. Dual gate oxide co-integrated devices with EOT 17Å/V_{dd} 1.1V and 29Å/V_{dd} 1.8V are reported. The interest of Ultra-Thin Buried Oxide substrates (UTBOX) is reported in term of Multiple Vt achievement and matching improvement. Delay improvement up to 15% is reported on Ring Oscillators as compared to bulk 45nm devices. In addition, for the first time 99.998% 2Mbit 0.374µm^2 SRAM cut functionality has been demonstrated. Thanks to a hybrid FDSOI/bulk co-integration with UTBOX all IP's required in a SOC are demonstrated for LP applications.

11:40 a.m.

28.7 16nm Functional 0.039mm2 6T-SRAM Cell with Nano Injection Lithography, Nanowire Channel, and Full TiN Gate (Late News), H.-Y. Chen, C.-C. Chen, F.-K. Hsueh, J.-T. Liu, C.-Y. Shen, C.-C. Hsu, S.-L. Shy, B.-T. Lin, H.-T. Chuang, C.-S. Wu, C. Hu*, C.-C. Huang and F.-L. Yang, National Nano Device Laboratories, *University of California, Berkeley

Record area size of 0.039µm2 for a functional 6T-SRAM cell has been successfully achieved with a novel Nano Injection Lithography (NIL) technique and dynamic V_{dd} regulator (DVR). The NIL technique is not only maskless for minimizing entry cost but also photoresist free to greatly enhance pattern resolution, down to 2nm 3-sigma line width roughness, and without significant proximity effect. Devices with nanowire channels and full TiN single gate for both N- and P-MOS are demonstrated with short channel and simplified integration process. This work discloses a new way to explore 16nm CMOS device and circuit design, and obtains early access to extreme CMOS scaling.

11:55 a.m.
28.8 Trigate 6T SRAM Scaling to 0.06 µm^2 (Late News), M. Guillorn, J. Chang, A. Pyzyna, S. Engelmann, E. Joseph, B. Fletcher, C. Cabral, Jr., C.-H. Lin, A. Bryant, M. Darnon, J. Ott, C. Lavoie, M. Frank, L. Gignac, J. Newbury, C. Wang, D. Klaus, E. Kratschmer, J. Bucchignano, B. To, W. Graham, I. Lauer, E. Sikorski, S. Carter, V. Narayanan, N. Fuller, Y. Zhang and W. Haensch, IBM T.J. Watson Research Center

We present an aggressively scaled trigate device architecture with undoped channels, high-κ gate dielectric, a single work function metal gate and novel BEOL processing yielding 6T SRAM bit cells as small as 0.06 µm2. This is the smallest SRAM cell demonstrated to date and represents the first time an SRAM based on a multi-gate FET (MUGFET) architecture has surpassed SRAM density scaling demonstrated with planar devices.

Session 29: Process Technology – Si Channel Engineering and Ge Technologies
Wednesday, December 9, 9:00 a.m.
Key Ballrooms 3, 4 and 6
Co-Chairs: *Robert Wallace, University of Texas at Dallas*
Kentaro Shibahara, Hiroshima University

9:00 a.m.
Introduction

9:05 a.m.
29.1 Steep Channel Profiles in n/pMOS Controlled by Boron-doped Si:C Layers for Continual Bulk-CMOS Scaling, A. Hokazono, H. Itokawa, I. Mizushima, S. Kawanaka, S. Inaba, Y. Toyoshima, Toshiba Corporation

B-doped-Si+Si:C+Si Epi-channel structure was proposed in order to form steep channel profiles both in nMOS and pMOS for the first time. This structure enhances the current drive by 15 ~ 18% in scaled CMOS down to 20 nm gate length.

9:30 a.m.

29.2 First CMOS Integration of Ultra Thin Body and BOX (UTB^2) Structures on Bulk Direct Silicon Bonded (DSB) Wafer with Multi-Surface Orientations, G. Bidal[1], F. Boeuf[1], S. Denorme[1], C. Laviron[3], K. Bourdelle[4], N. Loubet[1], Y. Campidelli[1], R. Beneyton[1], H. Moriceau[3], F. Fournel[3], P. Morin[1], S. Barnola[3] , T. Salvetat[3], P. Perreau[3], P. Gouraud[1], F. Leverd[1], B. Le-Gratiet[1], J.L. Huguenin[1], D. Fleury[1], K. Kusiaku[1], A. Cros[1], C. Leyris[1], S. Haendler[1], C. Borowiak[1], L. Clement[1], R. Pantel[1], G. Ghibaudo[2], T. Skotnicki[1], [1]STMicroelectronics, [2]IMEP-LAHC, [3]CEA-LETI , [4]SOITEC

For the first time we demonstrate the CMOS integration of undoped fully-depleted Ultra Thin Body and BOX devices (UTB^2) with (110)/(100) substrate crystal orientation for pFET and nFET respectively. For this, we used an original 3D-folded Bulk+/Silicon-On-Nothing (SON) process on DSB substrate. Resulting multi-surface orientations devices are studied.

9:55 a.m.

29.3 High Performance GeO_2/Ge nMOSFETs with Source/Drain Junctions Formed by Gas Phase Doping, K. Morii, T. Iwasaki, R. Nakane, M. Takenaka*, S. Takagi, The University of Tokyo, *also with JST-PRESTO

We demonstrated the n+/p junctions in Ge with low arsenic diffusion constant and low leakage current by using MOVPE-based gas phase doping. By combining the gas phase doping with GeO_2/Ge MOS interfaces, Ge nMOSFETs with the record high electron mobility of 804 cm^2/Vs have been demonstrated with high I_{on}/I_{off} ratio.

10:20 a.m.

29.4 High Performance n-MOSFETs with Novel Source/Drain on Selectively Grown Ge on Si for Monolithic Integration, H.-Y. Yu, M. Kobayashi, W.S. Jung, A.K. Okyay*, Y. Nishi, K.C. Saraswat, Stanford University, *Bilkent University

We demonstrate high performance Ge n-MOSFETs with novel raised source/drain fabricated on high quality Ge selectively grown on Si. S/D regions are formed by in-situ doping process for very low series resistance and abrupt and shallow junctions. The highest I_{on} for (100) Ge n-MOSFETs to-date is achieved with excellent I_{on}/I_{off} ratio($4x10^3$) and high I_{on}(3.23µA/µm).

10:45 a.m.

29.5 A Comprehensive Study of $Ge_{1-x}Si_x$ on Ge for the Ge nMOSFETs with Tensile Stress, Shallow Junctions and Reduced Leakage, G.-L. Luo, S.-C. Huang, C.-T. Chung*, D. Heh, C.-H. Chien, C.-C. Cheng*, Y.-J. Lee, W.-F. Wu, C.-C. Hsu, M.-L. Kuo, J.-Y. Yao, M.-N. Chang, C.-W. Liu, C, Hu, C.-Y. Chang*, F.-L. Yang, National Nano Device Laboratories, *National Chiao-Tung University, National Taiwan University, University of California

For the first time, growth of high-quality Ge-rich Ge1-xSix (0≤x≤0.14) layers on Ge substrate was demonstrated. An effective suppression of the phosphorus diffusion in Ge1-xSix and a better thermal stability of the nickel germanide on Ge1-xSix were observed. A higher rectifying ratio with a reduced diode leakage current in n+-$Ge_{1-x}Si_x$/p-$Ge_{1-x}Si_x$ is compared with n^+-Ge/p-Ge. These results indicate that it is suitable for $Ge_{1-x}Si_x$ to be used as source/drain (S/D) to fabricate the uniaxial tensile-strained channel Ge nMOSFETs.

11:10 a.m.
29.6 Comprehensive Study of GeO_2 Oxidation, GeO Desorption and GeO_2-Metal Interaction – Understanding of Ge Processing Kinetics for Perfect Interface Control-, K. Kita*, S.K. Wang, M. Yoshida, C.H. Lee, K. Nagashio*, T. Nishimura*, A. Toriumi*, The University of Tokyo, *also with JST-CREST

The guideline to control Ge/GeO_2 stacks was proposed. The effects of oxygen pressure and temperature were investigated, especially from the view point of GeO desorption-induced defects. Mid-gap Dit was reduced down significantly thanks to the kinetic control. It was also clarified that metal/GeO_2 interface has a significant role to determine GeO_2 MIS band alignment.

Session 30: Modeling and Simulation – Noise and Fluctuations
Wednesday, December 9, 9:00 a.m.
Key Ballroom 5
Co-Chairs: *Paolo Fantini, Numonyx*
Klaus von Arnim, Infineon Technologies

9:00 a.m.
Introduction

9:05 a.m.
30.1 Compact Model for Layout Dependent Variability (Invited), H. Aikawa, T. Sanuki, A. Sakata, E. Morifuji, H. Yoshimura, T. Asami, H. Otani, H. Oyamatsu, Toshiba Corporation Semiconductor Company

We have established a compact model which deals with MOSFET characteristic variations arising from complicated design layouts used in 45 nm CMOS technology node. By taking interactions between basic layout dependences, the model has acquired high applicability and predictability, which is verified by direct measurement of standard cells.

9:30 a.m.
30.2 Statistical Enhancement of Combined Simulations of RDD and LER Variability: What Can Simulation of a 10^5 Sample Teach Us?, D. Reid, C. Millar, G. Roy, S. Roy, A. Asenov, University of Glasgow

Analysis of 100,000 simulations of combined RDD and LER variability has shown that the distribution of V_t matches the distribution obtained by mathematically combining the individual distributions. Methods for the statistical enhancement of RDD and LER simulations are presented and the accuracy of the methods is examined.

9:55 a.m.
30.3 Design Space and Scalability Exploration of 1T-1STT MTJ Memory Arrays in the Presence of Variability and Disturbances, A. Raychowdhury, D. Somasekhar, T. Karnik, V. De, Intel Corporation

This paper presents modeling and analysis of 1T-1MTJ STTRAM memory arrays under process variation and thermal disturbances. Bounds on the magnetic material design space for aggressive embedded applications have been shown. Impact of relaxed timing/area and the effect of scaling for 1T-1MTJ bitcells have been evaluated.

10:20 a.m.
30.4 Impact of Interface States on MOS Transistor Mismatch, P. Andricciola, H.P. Tuinhout, B. De Vries, N.A.H. Wils, A.J. Scholten, D.B.M. Klaassen, NXP Semiconductor

Statistical device simulations show that interface states fluctuating in terms of density, position and energy, have an enormous impact on mismatch fluctuations in sub-threshold. Through a new analysis method, based on mismatch signature and PCA, it is demonstrated that interface states should not be neglected for modern MOSFET mismatch modeling.

10:45 a.m.
30.5 Statistical Model for MOSFET Low-Frequency Noise under Cyclo-Stationary Conditions, G. Wirth, R. da Silva P. Srinivasan*, J. Krick*, R. Brederlow*, UFRGS, *Texas Instruments

A statistical model for the low-frequency noise behavior of MOSFETs under cyclo-stationary excitation is presented. The model is based on discrete device physics quantities, which are shown to cause statistical variability in LF noise behavior. Good agreement between experimental data, Monte Carlo simulations and model is demonstrated.

11:10 a.m.

30.6 Compact Modeling of Flicker Noise Variability in Small Size MOSFETs, T.H. Morshed, M.V. Dunga, J. Zhang, D.D. Lu, A.M. Niknejad, C. Hu, University of California, Berkeley

A statistical compact model of flicker noise in scaled MOSFETs is presented, providing device size dependent noise mean and standard deviation. The model is verified with Monte Carlo simulation and experimental data. Our discovery that flicker noise exhibits log normal distribution is utilized to construct a compact model that allows designers to specify the sizes and desired % yields of critical devices when performing SPICE simulation of circuit performance.

11:35 a.m.

30.7 Distributed-Poole-Frenkel Modeling of Anomalous Resistance Scaling and Fluctuations in Phase-Change Memory (PCM) Devices, D. Fugazza, D. Ielmini, S. Lavizzari, A.L. Lacaita, Politecnico di Milano

A new distributed Poole-Frenkel conduction model for the active chalcogenide material in phase change memory is presented, accounting for anomalous resistance scaling and current fluctuations. Calculation results agree with experimental data and allow for scaling projections at nodes F = 45 - 8 nm for resistance window and signal-to-noise ratio.

Session 31: Characterization, Reliability and Yield – BTI and Memory
Wednesday, December 9, 9:00 a.m.
Key Ballroom 1 and 2
Co-Chairs: Kiyoshi Takeuchi, NEC Electronics Corp.
Zsolt Tokei, IMEC

9:00 a.m.
Introduction

9:05 a.m.
31.1 Switching Oxide Traps as the Missing Link Between Negative Bias Temperature Instability and Random Telegraph Noise, T. Grasser, H. Reisinger*, W. Goes, T. Aichinger**, P. Hehenberger^, P.-J. Wagner, M. Nelhiebel*, J. Franco^, B. Kaczer^, TU Wien, *Infineon, **KAI, ^IMEC

We demonstrate both theoretically and experimentally that random telegraph noise and the recoverable component of NBTI are due to charge trapping in switching oxide traps. Most importantly, the capture and emission times of the defects are uncorrelated, revealing explicitly that individual defects constitute the recovery of NBTI.

9:30 a.m.
31.2 On the Differences Between Ultra-fast NBTI Measurements and Reaction-Diffusion Theory, A.E. Islam, S. Mahapatra*, S. Deora*, V.D. Maheta*, M.A. Alam, Purdue University, *IIT Bombay

We use a single hole-trapping/interface-trap decomposition framework to demonstrate that the start of interface-trap relaxation is generally consistent with the Reaction-Diffusion theory. Our analysis, for the first time, explains nitrogen, temperature, stress-time, duty-cycle dependence of AC/DC ratio for nitrided transistors, which should be extremely important for NBTI AC analysis.

9:55 a.m.

31.3 Can the Reaction-Diffusion Model Explain Generation and Recovery of Interface States Contributing to NBTI?, Z. Teo, D.S. Ang, K.S. See*, Nanyang Technological University, *Chartered Semi-conductor Manufacturing

By addressing measurement artifacts relating to oxide traps via ultrafast charge pumping, new evidences for interface state generation (dNit), which do not conform to a diffusion or dispersive transport model, are presented. It is shown that dNit is relatively permanent and its power-law time exponent is consistently ~0.27 over a wide gate voltage and temperature range.

10:20 a.m.

31.4 New Degradation Mechanisms and Reliability Performance in Tunneling Field Effect Transistors, G.F. Jiao, Z.X. Chen**, H.Y. Yu**, X.Y. Huang, D.M. Huang, N. Singh*, G.Q. Lo*, D.-L. Kwong*, M.-F. Li, Fudan University, *Institute of Microelectronics, **also with Nanyang Technological University

Tunneling n-FET reliability performance is studied by physical analysis and experimental measurements. (1) A new degradation mechanism by interface traps induced change of tunneling field and current Id is demonstrated.(2) Under PBTI or HC stress, there is a strong peak of vertical field Ex at the source/overlapping region, inducing high interface trap degradation, due to P+ doping of the source. These explains the large PBTI and HC degradation, very different from those observed in conventional n-MOSFETs.

10:45 a.m.

31.5 Reliability of Barrier Engineered Charge Trapping Devices for Sub-30nm NAND Flash (Invited), R. Liu, H.-T. Lue, K.C. Chen, C.-Y. Lu, Macronix International Co. Ltd

Charge trapping kinetics and the impact of edge field induced degradation are clarified. Performance enhancement such as hemi-cylindrical shape and high-K/metal-gate and their impact on reliability are investigated. Finally, issues for extreme scaling to below 20nm nodes, such as few-electron data retention and random telegraph noise, are examined.

11:10 a.m.

31.6 Resolving Fast V_{TH} Transients After Program/Erase of Flash Memory Stacks and Their Relation to Electron and Hole Defects, M. Toledano-Luque, R. Degraeve*, M.B. Zahid*, B. Kaczer*, J. Kittl*, M. Jurczak*, G. Groeseneken*, J. Van Houdt*, Universidad Complutense de Madrid, *IMEC

A new fast technique is developed to investigate the short term post program and erase discharge of flash memory devices based on high-k dielectrics. The procedure is based on fast VTH-evaluation methods developed on NBTI and provides the transient characteristics after 20ms under program or erase conditions instead of the usual transients registered after 1s.

11:35 a.m.
31.7 Understanding Amorphous States of Phase-Change Memory Using Frenkel-Poole Model, Y.H. Shih, M.H. Lee, M. Breitwisch*, R. Cheek*, J.Y. Wu, B. Rajendran*, Y. Zhu*, E.K. Lai, C.F. Chen, H.Y. Cheng, A. Schrott*, E. Joseph*, R. Dasaka*, S. Raoux*, H.L. Lung, C. Lam*, Macronix International Co. Ltd., *IBM TJ Watson Research Center

A method based on Frenkel-Poole emission is proposed to model the amorphous state (high resistance state) in mushroom-type phase- change memory devices. The model provides unique insights to probe the device after amorphizing (RESET) operation. Even when the resistance appears the same under different RESET conditions, our model suggests that both the amorphous region size and the defect states are different. With this powerful new tool detailed changes inside the amorphous GST for MLC operation and retention tests are revealed.

Session 32: Characterization, Reliability and Yield – Random Telegraph Noise
Wednesday, December 9, 1:30 p.m.
Holiday Ballrooms 1, 2 and 3
Co-Chairs: *Xavier Garros, CEA LETI/MINATEC*
Jurriaan Schmitz, University of Twente

1:30 p.m.
Introduction

1:35 p.m.
32.1 New Analysis Methods for Comprehensive Understanding of Random Telegraph Noise, T. Nagumo, K. Takeuchi, S. Yokogawa, K. Imai, Y. Hayashi, NEC Electronics Corporation

Two methods useful for comprehensive understanding of random telegraph noise are proposed: time lag plot and a model-based statistical parameter extraction scheme. Dependence of trap number on V_{gs} is caused by the modulation of time constant by V_{gs}. Modeling of undetectable traps is important for product reliability evaluation.

2:00 p.m.
32.2 Characterization of Oxide Traps Leading to RTN in High-k and Metal Gate MOSFETs, S. Lee, H.-J. Cho, Y. Son, D.S. Lee, H. Shin, Seoul National University

We propose a new method to characterize oxide traps in high-k dielectric devices. For the first time, all the cases that the trap is located either in high-k dielectric layer or interfacial layer and electron tunneling either from the channel or the gate electrode are considered in the method.

2:25 p.m.
32.3 Impact of Random Telegraph Signals on V_{min} in 45nm SRAM, S.O. Toh, Y. Tsukamoto*, Z. Guo, L. Jones, T.-J. King Liu, B. Nikolic, University of California, Berkeley, *Renesas Technology Corp.

A new measurement technique to accelerate RTS testing is presented. Measurements of RTS amplitudes in 45nm SRAM transistor Ids and cell write margin show a complex dependence of write margin on RTS in multiple transistors. Statistical analysis indicates that fail bit rate and Vmin degradation due to RTS is small.

2:50 p.m.
32.4 Reduction of Random Telegraph Noise in High-*k*/Metal-gate Stacks for 22 nm Generation FETs, N. Tega, H. Miki, Z. Ren***, C.P. D'Emic**, Y. Zhu**, D.J. Frank**, J. Cai**, M.A. Guillorn**, D.-G. Park**, W. Haensch**, K. Torii*, Hitachi America Ltd., *Hitachi Ltd., **IBM TJ Watson Research Center, ***IBM SRDC

This work demonstrates, for the first time, the reduction of random telegraph noise (RTN) in high-*k*/metal gate (HK/MG) stacks incorporated in 22 nm generation FETs. Moreover, based on a statistical comparison of fabricated FETs, RTN ΔV_{th} of HK FETs is smaller than for SiON FETs due mostly to fewer traps and partly to thinner T_{inv} in HK/MG. Therefore, RTN impact may not exceed random dopant fluctuation impact until the 15 nm generation and beyond.

3:15 p.m.
32.5 Effect of Bottom Electrode of ReRAM with Ta_2O_5/TiO_2 Stack on RTN and Retention, M. Terai, Y. Sakotsubo, Y. Saito, S. Kotsuji, H. Hada, NEC Corporation

Effect of bottom electrode of ReRAM with Ta_2O_5/TiO_2 stack on noise and thermal stability was investigated. The current fluctuation due to complex random telegraph noise caused erroneous read out operation especially for multi-level operation. Stack using Ru or Pt electrode without Ti diffusion achieved low noise and high thermal stability.

3:40 p.m.

32.6 A New and Simple Experimental Approach to Characterizing the Carrier Transport and Reliability of Strained CMOS Devices in the Quasi-Ballistic Regime, E.R. Hsieh, S.S. Chung, P.W. Liu*, W.T. Chiang*, C.H. Tsai*, W.Y. Teng*, C.I. Li*, T.F. Kuo*, Y.R. Wang*, C.L. Yang*, C.T. Tsai*, G.H. Ma*, National Chiao Tung University, *United Microelectronics Corporation

A new $V_{D,sat}$ method, without complicate temperature measurement setup, has been developed to study the transport characteristics of MOSFETs in the quasi-ballistic regime. It showed good match with that of Temperature Dependent Method (TDM) from the quantum theory. The carrier transport properties after HC stress were also examined. It was found stress induced variation of B_{sat} dominates $I_{D,sat}$ degradation. Moreover, for the study on strain-CMOS devices, the drain current enhancement is strongly related to V_{inj}, a good monitor for the strain design. While, considering the devices after the HC stress, ballistic efficiency, Bsat is responsible for the ID degradation. A roadmap of the V_{inj} from reported results has also been provided.

Session 33: Displays, Sensors and MEMS – Micro-Resonators and RF MEMS
Wednesday, December 9, 1:30 p.m.
Holiday Ballroom 6
Co-Chairs: *Farrokh Ayazi, Georgia Institute of Technology*
Sunil Bhave, Cornell University

1:30 p.m.
Introduction

1:35 p.m.

33.1 Temperature Compensated Solidly Mounted Bulk Acoustic Wave Resonators with Optimum Piezoelectric Coupling Coefficient, M.A. Allah, J. Kaitila*, R. Thalhammer*, W. Weber*, D. Schmitt-Landsiedel, Technical University of Munich, *Infineon Technologies AG

Through a new method of temperature compensation, fully compensated, high coupling coefficient and high Quality factor solidly mounted bulk acoustic wave resonators are fabricated working at 2.45GHz. From the compensated resonators a new value for the temperature coefficient of elasticity of sputtered thin film SiO2 layers is determined.

2:00 p.m.
33.2 Temperature Compensation of Silicon Micromechanical Resonators via Degenerate Doping, A.K. Samarao, F. Ayazi, Georgia Institute of Technology

This work presents degenerate doping of a silicon micromechanical resonator as a new method to compensate resonator temperature coefficient of frequency (TCF). The TCF of a 100 MHz silicon bulk acoustic resonator is reduced from -29 ppm/°C to -3.56 ppm/°C using degenerate boron doping and to -2.72 ppm/°C using boron-assisted aluminum doping while maintaining a quality factor (Q) of 18000 in air.

2:25 p.m.
33.3 Self-Sustained Low Power Oscillator Based on Vibrating Body Field Effect Transistor, D. Grogg, S. Ayoz, A.M. Ionescu, Ecole Polytechnique Fédérale de Lausanne

The operation of a vibrating body field effect transistor (VB-FET) near pull-in is exploited to experimentally demonstrate a self-oscillating device without the presence of an external feedback loop. The positive feedback mechanism is triggered at the onset of weak inversion in a depleted VB-FET channel.

2:50 p.m.

33.4 BEOL Embedded RF-MEMS Switch for mm-Wave Applications, M. Kaynak, K.E. Ehwald, J. Drews, R. Scholz, F. Korndorfer, D. Knoll, B. Tillack, R. Barth, M. Birkholz, K. Schulz, Y.M. Sun, D. Wolansky, S. Leidich*, S. Kurth*, Y. Gurbuz**, IHP, *Fraunhofer Research Institution for Electronic Nano Systems, **Sabanci University Orhanli

An RF-MEMS capacitive switch for mm-wave integrated circuits was fabricated for the first time by embedded integration in a BiCMOS Back-End-of-Line (BEOL). The capacitance ratio (coff/con) is measured as 1:10 while insertion loss and isolation performances are found to fall below 1.65dB and to exceed 15dB, respectively, in the frequency range of 60GHz to 110GHz.

3:15 p.m.

33.5 Low-Loss MEMS Band-Pan Filters with Improved Out-of-Band Rejection by Exploiting Inductive Parasitics, Y. Shim, R. Tabrizian*, F. Ayazi*, M. Rais-Zadeh, University of Michigan, Ann Arbor, *Georgia Institute of Technology

Fixed and tunable bandpass filters are implemented using silver to achieve high performance. Inductive parasitics are exploited to improve the out-of-band rejection. The properties of several fabricated filters are discussed. An insertion loss of better than 2.9dB has been achieved for filters across 20MHz to 640MHz on silicon. Out-of-band rejection of filters is as high as 60dB.

3:40 p.m.
33.6 Highly Tunable Band-Stop Filters Based on AIN RF MEM Capacitive Switches with Inductive Arms and Zipping Capacitive Coupling, M. Fernandez-Bolanos, T. Lisec*, C. Dehollain, D. Tsamados, P. Nicole**, A.M. Ionescu, Ecole Polytechnique Fédérale de Lausanne, *Fraunhofer-Institut fur Siliziumtechnologie, **THALES Airborne Systems

This paper presents a miniature single device wideband tunable band-stop filter working in the K-band frequencies and thermally stable for space and airborne applications. An outstanding 55% tuning range is achieved thanks to the added tunability of the MEMS capacitive switch (with a continuous quasi-linear tuning range of 20%) and the voltage-controlled capacitance coupling zipping effect of the meander arm inductance when approaching to the substrate. Two band-stop filters have been designed for 13.5-29.5GHz and 17-37GHz frequency range resulting in rejection levels of -15 dB/-20 dB for the whole tuning range and pass band insertion loss of -0.19 dB/-0.25 dB at 10GHz, respectively.

4:05 p.m.
33.7 Design and Reliability of a Micro-Relay Technology for Zero-Standby-Power Digital Logic Applications, H. Kam, V. Pott, R. Nathanael, J. Jeon, E. Alon, T.-J. King Liu, University of California, Berkeley

A pathway to enable reliable micro-relays for digital logic applications through proper contact design is proposed and demonstrated with TiO_2-coated W contacting electrodes. The static and dynamic behavior of these relays is well modeled by the lumped parameter model. Scaled relays appear promising for ultra-low-power applications requiring performance up to ~100MHz.

4:30 p.m.
33.8 Body-Biased Complementary Logic Implemented Using AlN Piezoelectric MEMS Switches, N. Sinha, T. Jones, Z. Guo, G. Piazza, University of Pennsylvania

The paper reports on the first implementation of a low voltage complementary inverter (< 1.5 V) by using body-biased aluminum nitride piezoelectric MEMS switches. n and p-type mechanical transistors with low threshold voltage (30 mV), fast switching speed (220 ns) and low subthreshold slope (< 1mV/dec) have been demonstrated.

Session 34: Memory Technology – Flash Memory
Wednesday, December 9, 1:30 p.m.
Key Ballrooms 7, 9 and 10
Co-Chairs: Tzu-Ning Fang, Spansion
Jan Van Houdt, IMEC

1:30 p.m.
Introduction

1:35 p.m.
34.1 Investigation of Ballistic Current in Scaled Floating-Gate NAND FLASH and a Solution, S. Raghunathan, T. Krishnamohan, K. Parat*, K. Saraswat, Stanford University, *Intel Corp.

For the first time, we investigate the ballistic transport that occurs across ultra-thin (fabricated upto 7nm) poly-Si FGs in scaled NAND FLASH and experimentally determine mean-free-path. We also demonstrate a solution using ultra-thin metal FG(fabricated upto 3nm) and show 1000X lesser ballistic current than poly-Si of same thickness.

2:00 p.m.

34.2 The New Program/Erase Cycling Degradation Mechanism of NAND Flash Memory Devices, A. Fayrushin, K.S.Seol, J.H. Na, S.H. Hur, J.D. Choi, K. Kim, Samsung Electronics

Program/erase degradation model based on non-uniformly distributed trapped charge in tunnel oxide is suggested to explain midgap voltage and subthreshold slope change observed during program/erase cycling of current Flash memory. The model is supported by device structure analysis, experimental and simulation work.

2:25 p.m.

34.3 A Novel Planar Floating-Gate (FG) / Charge-Trapping (CT) NAND Device Using BE-SONOS Inter-Poly Dielectric (IPD), H.-T. Lue, P.-Y. Du, T.-H. Hsu, Y.-H. Hsiao, S.-C. Lai, S.-Y. Wang, S.P. Hong, M.T. Wu, F.H. Hsu, N.Z. Lien, C.-P. Lu, J.-Y. Hsieh, L.-W. Yang, T. Yang, K.-C. Chen, K.-Y. Hsieh, R. Liu, C.-Y. Lu, Macronix International Co. Ltd.

We propose a completely new approach for NAND Flash scaling- a planar FG using a trapping IPD for storage. Our concept is to combine the merits of CT and FG – CT for good retention and scaling to few-electron regime and FG for edge effect immunity and faster erase. The planar "fusion" FG/CT devices are fabricated by replacing the conventional IPD ONO of a FG device by a CT BE-SONOS structure. Both simulation and experimental results indicate that most of the stored electrons are trapped inside the nitride instead of the FG. The CT storage provides excellent retention even for a very thin tunnel oxide (<5nm). On the other hand, the thin FG provides an equi-potential channel that screens any non-uniform injection effect.

2:50 p.m.
34.4 Reliability Improvement in Planar MONOS Cell for 20nm-node Multi-Level NAND Flash Memory and Beyond, W. Sakamoto, T. Yaegashi, T. Okamura, T. Toba, K. Komiya, K. Sakuma, Y. Matsunaga, Y. Ishibashi, H. Nagashima, M. Sugi, N. Kawada, M. Umemura, M. Kondo, T. Izumida, N. Aoki, T. Watanabe, Toshiba Corporation

20nm-node planar MONOS cell which has improved reliability is developed. Extremely wide program/erase Vth window and good retention characteristics after cycling stress are obtained by buried charge cell structure. The buried charge planar MONOS cell is suitable for Flash memory with 20nm-node and beyond.

3:15 p.m.
34.5 Potential Well Engineering by Partial Oxidation of TiN for High-Speed and Low-Voltage Flash Memory with Good 125°C Data Retention and Excellent Endurance, G. Zhang*, C.H. Ra*, H.-M. Li, C. Yang, W.J. Yoo, Sungkyunkwan University, *also with Korea Institute of Science and Technology

Potential well engineering is proposed for NAND Flash memory. The engineered well (EW) has a variable tunnel barrier. It switches the P/E and retention modes by EW transformation, and it is insensitive to tunnel barrier degradation. It enables fast program (<us), good data retention at 125°C and excellent endurance (>10E7).

3:40 p.m.
34.6 Understanding STI Edge Fringing Field Effect on the Scaling of Charge-Trapping (CT) NAND Flash and Modeling of Incremental Step Pulse Programming (ISPP), H.-T. Lue, T.-H. Hsu, Y.-H. Hsiao, S.-C. Lai, E.-K. Lai, S.-P. Hong, M.-T. Wu, F.-H. Hsu, N.Z. Lien, C.-P. Lu, S.-Y. Wang, J.-Y. Hsieh, L.-W. Yang, T. Yang, K.-C. Chen, K.-Y. Hsieh, R. Liu, C.-Y. Lu, Macronix International Co. Ltd.

The impact of edge fringing field effect on charge-trapping (CT) NAND Flash with various STI structures is extensively studied for a thorough understanding. First, we find that the edge fringing field can cause abnormal subthreshold current during programming. Second, the edge fringing field effect significantly changes the P/E speed and degrades the incremental-step-pulse programming (ISPP) slope from ideal value (=1). By using 3D simulation we found that the edge fringing field greatly degrades the tunnel oxide electric field, and more charge injection is required to obtain the same memory window. We propose an analytical ISPP model and successfully simulate various STI structures.

4:05 p.m.
34.7 Program Charge Effect on Random Telegraph Noise Amplitude and Its Device Structural Dependence in SONOS Flash Memory, J.P. Chiu, Y.L. Chou, H.C. Ma, T. Wang, S.H. Ku*, N.K. Zou*, V. Chen*, W.P. Lu*, K.C. Chen*, C.-Y. Lu*, National Chiao-Tung University, *Macronix International Co. Ltd.

Nitride program charge effect on the amplitude of random telegraph noise in SONOS flash cells is investigated. We measure and simulate RTN amplitudes in floating gate flash, planar SONOS, and FinFET SONOS cells. We find that a planar SONOS has a wide spread in RTN amplitudes after programming due to a current-path percolation effect caused by random discrete nitride charges. The RTN amplitude spread can be significantly reduced in surrounding gate SONOS.

Session 35: Quantum, Power and Compound Semiconductors – CMOS Compatible, High Mobility III-V Devices
Wednesday, December 9, 1:30 p.m.
Key Ballrooms 8, 11 and 12
Co-Chairs: Kei May Lau, Hong Kong University of Science and Technology
Tomas Palacios, Massachusetts Institute of Technology

1:30 p.m.
Introduction

1:35 p.m
35.1 High-Performance InSb Based Quantum Well Field Effect Transistors for Low-Power Dissipation Applications (Invited), T. Ashley, M. Emeny, D. Hayes, K. Hilton, R. Jefferies, J. MacIean, S.Smith, A. Tang, D. Wallis and P. Weber, QintiQ

Indium antimonide (InSb) has the highest electron mobility and saturation velocity of any conventional semiconductor, giving potential for a range of analogue and digital ultra-high speed, low power dissipation applications. N-channel quantum well FETs have been fabricated with current gain cut-off frequency (f_T) of more than 250 GHz and power gain cut-off frequency (f_{max}) of 500 GHz. Outline designs confirm the potential for multi-stage low noise amplifiers operating at more than 200 GHz, for applications such as integrated passive millimetre wave imaging.

2:00 p.m.
35.2 Monolithic Integration of InSb Hall-Effect Devices with Si LSI on Si Substrate, Y. Kunimi, A. Sakurai, S. Akiyama, H. Fujita, Y. Shibata, K. Nagakura, Y. Noma, T. Yamamoto, Y. Yamaha, Asahi-KASEI Microdevices Corporation

This paper describes for the first time, monolithic integration of high quality InSb Hall device with Si-LSI. Hall device was connected to Si-LSI with metal and controlled by Si-LSI. Temperature drift of output voltage from Hall device could be made within 2% during wide temperature range (from -40C to 125C).

2:25 p.m.

35.3 Engineering of Strained III-V Heterostructures for High Hole Mobility, A. Nainani, S. Raghunathan, D.Witte, M. Kobayashi, T. Irisawa, T. Krishnamohan*, K. Saraswat, B.R. Bennett**, M. Ancona**, J.B. Boos**, Stanford University, *Intel Corp., **Naval Research Lab

Modeling is used to predict optimum channel/strain for high hole-mobility in III-V HFETs. Two heterostructures with strained Sb-based channels are analyzed. m* and energy splitting between light/heavy hole bands with strain is quantified. For $In_{.41}$GaSb/GaSb highest reported hole-mobilities >3X compared to uniaxially strained-Si at 7E12 sheet charge are experimentally demonstrated.

2:50 p.m.

35.4 Extraction of Virtual-Source Injection Velocity in Sub-100 nm III-V HFETs, D.-H. Kim, J.A del Alamo, D.A. Antoniadis, B. Brar*, Massachusetts Institute of Technology, *TSC

We propose a rigorous extraction of the source injection velocity in III-V HFETs. Sub-100 nm devices exhibit velocity $> 3 \times 10^7$ cm/s at $V_{dd} = 0.5$ V, which is 2 times that of Si nFETs. We also perform a physical modeling which yields velocity consistent with those obtained experimentally.

3:15 p.m.
35.5 New Insight into Fermi-Level Unpinning on GaAs: Impacts of Different Surface Orientations, M. Xu, K. Xu, R. Contreras*, M. Milojevic*, T. Shen, O. Koybasi, Y.Q. Wu, R.M. Wallace*, P.D. Ye, Purdue University, *University of Texas at Dallas

We systematically study NMOSFETs, MOSCAPs, and interfacial chemistry on GaAs (100), (110), (111)A and (111)B four different crystalline surfaces. With direct ALD Al_2O_3, we can particularly achieve much higher drain current on GaAs(111)A NMOSFET compared to that on the other 3 surfaces. Also, the results of MOSCAPs and interfacial chemistry obtained on (111)A surface are astonishingly different from those on (111)B, (110) and (100) surfaces. These experimental results conclusively demonstrate that Fermi-level on GaAs (111)A surface is indeed unpinned with a direct ALD Al_2O_3 interface and Fermi-level pinning is not an intrinsic property of GaAs.

Session 36: Process Technology – Advanced Interconnect Technologies for CMOS Applications
Wednesday, December 9, 1:30 p.m.
Key Ballrooms 3, 4 and 6
Co-Chairs: *Paul Ferreira, STMicroelectronics*
Naoya Inoue, NEC Electronics

1:30 p.m.
Introduction

1:35 p.m.
36.1 Optimization of Metallization Processes for 32-nm-node Highly Reliable Ultralow-k (k=2.4)/Cu Multilevel Interconnects Incorporating a Bilayer Low-k Barrier Cap (k=3.9), M. Iguchi, S. Yokogawa, H. Aizawa, Y. Kakuhara, H. Tsuchiya, N. Okada, K. Imai, M. Tohara*, K. Fujii*, T. Watanabe*, NEC Electronics Corporation, *Toshiba Corporation

We demonstrated that reliability of 32-nm-node technology can be improved without excessive wiring resistance by using CuAl seed technology with high-temperature and short time annealing. Though the increase of the wiring resistivity was about 10%, the reliability about EM and SiV was clearly improved by using Cu-0.5wt%Al seed metal.

2:00 p.m.
36.2 Feasibility Study of 70nm Pitch Cu/Porous Low-k D/D Integration Featuring EUV Lithography Toward 22nm Generation, N. Nakamura, N. Oda, E. Soda, N. Hosoi, A Gawase, H. Aoyama, Y. Tanaka, D. Kawamura, S. Chikaki, M. Shiohara, N. Tarumi, S. Kondo, I. Mori, S. Saito, SELETE

A feasibility study of 70 nm pitch 2-level dual-damascene interconnects featuring EUV lithography is presented. Using Ru barrier metal, a low resistivity below 4.5 μΩcm was obtained. The predicted circuit-performance using the scalable porous silica (k=2.1) was 8% higher than that with porous-SiCO (k=2.65). The reliability in 22 nm generation was consistent with previous generations.

2:25 p.m.
36.3 Top-Gated FETs/Inverters with Diblock Copolymer Self-Assembled 20 nm Contact Holes, L.-W. Chang, T.L. Lee*, C.H. Wann*, C.Y. Chang*, H.-S.P. Wong, Stanford University, *TSMC

We have successfully fabricated FETs with 20 nm contact holes patterned using self-assembled diblock copolymer. Alignment of the self-assembled contact holes to the MOSFET source and drain is achieved with a unique guiding layer. The self-assembly process is integrated with an existing CMOS process flow using conventional tools on a full wafer level. This is the first demonstration of top-gated FET fabricated using self-assembly at the (n+1)th level where $n \geq 1$.

2:50 p.m.

36.4 Chip-Level and Package-Level Seamless Interconnect Technologies for Advanced Packaging (Invited), S. Yamamichi, K. Mori, K. Kikuchi, H. Murai, D. Ohshima, Y. Nakashima, K. Soejima*, M. Kawano*, T. Murakami, NEC Corporation, *NEC Electronics Corporation

Seamless interconnect between LSI chip and package substrate is successfully developed for wafer and package levels. The chip-level seamless interconnect with thick Cu wiring is fabricated by resin CMP. The package-level seamless interconnect achieves extremely small thickness, low thermal resistance and fully-functional operation for microprocessor chip, using Cu base plate.

3:15 p.m.

36.5 RF Performance Upgrading of Low-power 40nm-node CMOS Devices by Extremely Low-resistance Partially-thickened Local (PTL)-interconnects, K. Hijioka, J. Kawahara, M. Narihiro, I. Kume, A. Tanabe, H. Nagase, H. Yamamoto, N. Inoue, T. Takeuchi, T. Onodera, S. Saito, N. Furutake, Y. Hayashi, NEC Electronics Corporation

A new partially-thickened-local (PTL)-interconnect with an extremely low resistance is implemented into the 40nm-node low-power RF-CMOS. The PTL-interconnect featured by the Cu dual-damascene (DD) slit-contact (SLICT), accomplishes drastically reduction in the metal-1 and contact resistance. The maximum oscillation frequency of RF-MOSFET is pushed up 30% referred to that with W-pillar contacts. The low-resistance PTL interconnect backed with the Cu-DD SLICT is essential for low-power RF/mixed-signal SoCs.

Session 37: Modeling and Simulation – Emerging Devices
Wednesday, December 9, 1:30 p.m.
Key Ballroom 5
Co-Chairs: *Max Fischetti, University of Massachusetts*
Paulette Clancy, Cornell University

1:30 p.m.
Introduction

1:35 p.m.
37.1 Multilayer Graphene Nanoribbon for 3D Stacking of the Transistor Channel, Y. Ouyang, H. Dai*, J. Guo, University of Florida, *Stanford University

Simulations are performed to explore the possibility of boosting the ballistic on-current of GNRFETs by using the experimentally accessible multilayer GNR, which provides natural structures for 3D stacking of the transistor channel. The effects of the number of graphene layers and interlayer coupling strength are studied under different gating technologies.

2:00 p.m.
37.2 Physical Insights on Graphene Nanoribbon Mobility Through Atomistic Simulations, A. Betti, G. Fiori, G. Iannaccone, Y. Mao*, Universitá di Pisa, *Dana Farber Cancer Institute Pathology

This work uses atomistic simulations to gain physical understanding of the role played by different scattering mechanisms in limiting mobility in Graphene Nanoribbons FETs. Line edge roughness, single defects, ionized impurities, and acoustic and optical phonons are considered. Narrow graphene nanoribbons are expected to exhibit limited mobility.

2:25 p.m.
37.3 A Computational Evaluation of the Designs of a Novel Nanoelectromechanical Switch Based on Bilayer Graphene Nanoribbon, K.-T. Lam, G. Liang, National University of Singapore

A novel nanoelectromechanical switch based on bilayer graphene nanoribbon is proposed and its operating mechanism is briefly discussed. Three floating gate designs for the device are discussed for different applications and optimizing parameters such as gate capacitance and spring constant are used to tune the switching gate bias.

2:50 p.m.
37.4 Simulation Study of Switching Mechanism in Carbon-Based Resistive Memory with Molecular Dynamics and Extended Hückel Theory-Based NEGF Method, X. Guan, Y. He, L. Zhao, J. Zhang, Y. Wang, H. Qian, Z. Yu, Tsinghua University

Filament based switching mechanism of carbon-based resistive memory is studied on a fully atomistic level, using molecular dynamics simulation and the Extended-Hückel-Theory based NEGF method. Based on the geometry and temperature dependence of the intrinsic switching time, scaling trend, optimization parameters as well as trade-off strategy in cell design are discussed.

3:15 p.m.
37.5 1D Broken-Gap Tunnel Transistor with MOSFET-Like On-Currents and Sub-60mV/dec Subthreshold Swing, S.O. Koswatta*, S.J. Koester, W. Haensch, IBM TJ Watson Research Center, *also with University of Notre Dame

A novel tunneling field-effect transistor (TFET) concept based on one-dimensional broken-gap heterostructure geometry is proposed. Detailed quantum transport simulations show that MOSFET-like current-drive along with less than 60mV/decade subthreshold swing can be obtained in this device for high-performance circuit operation with low-power dissipation.

3:40 p.m.
37.6 Performance Comparisons of Tunneling Field-Effect Transistors made of InSb, Carbon, and GaSb-InAs Broken Gap Heterostructures, M. Luisier, G. Klimeck, Purdue University

In this paper we use one single atomistic, quantum mechanical device simulator based on the tight-binding approach to evaluate the performances of p-i-n, low direct band gap tunneling FETs. We focus on InSb, Carbon, and GaSb-InAs broken gap devices, with either one-dimensional or two-dimensional transport.

4:05 p.m.
37.7 A Non-iterative Compact Model for Carbon Nanotube FETs Incorporating Source Exhaustion Effects,
L. Wei, D.J. Frank*, L. Chang*, H.-S.P. Wong, Stanford University, *IBM TJ Watson Research Center

We present a new non-iterative compact model based on quantum capacitance for CNFETs, suitable for circuit simulation and optimization. The importance of source exhaustion is unveiled as a fundamental current limiter in ballistic transport. System level design optimization results show CNFET as a great candidate for very advanced technology nodes.

4:30 p.m.
37.8 Modeling and Optimization of Polymer based Bulk Heterojunction (BH) Solar cell, B. Ray, P.R. Nair, E. Garcia, M.A. Alam, Purdue University

In this paper, we present a theoretical/computational process/device model of polymer/fullerene organic bulk heterojunction (BH) solar cells to explore the coupled flow of exciton/electron/hole within the meso-structure of the cell and quantitatively relate -- possibly for the first time -- the process conditions to the performance of BH solar cell.

Session 38: Solid-State and Nanoelectronic Devices – Devices and Circuits Based on Nanowires and Solid-Electrolyte Switches
Wednesday, December 9, 1:30 p.m.
Key Ballrooms 1 and 2
Co-Chairs: *Andreas Schenk, ETH Zurich*
Franz Kreupl, SanDisk Corporation

1:30 p.m.
Introduction

1:35 p.m.
38.1 Nanowire Based Electronics: Challenges and Prospects (Invited), W. Lu, University of Michigan,

This review provides a survey of recent progresses in nanowire electronics. Studies at the single-device level have demonstrated that electrical integrity can be preserved in aggressively scaled devices, with performance matching or better than their CMOS counterparts. Three different approaches to address the circuit integration issue will also be presented.

2:00 p.m.
38.2 CMOS Compatible Ge/Si Core/Shell Nanowire Gate-All-Around pMOSFET Integrated with HfO_2/TaN Gate Stack, J.W. Peng, N. Singh, G.Q. Lo, D.L. Kwong, S.J. Lee*, Institute of Microelectronics, *National University of Singapore

Ge/Si core/shell gate-all-round nanowire pFET integrated with HfO_2/TaN gate stack is demonstrated using fully CMOS compatible process. Devices with 100 nm gate length achieved high ION of ~946 μA/μm at V_G - V_T = -0.7 V and V_{DS} = -1 V and on/off ratio of 10^4 with good decent subthreshold behavior. Significant improvement in hole mobility and ballistic efficiency is demonstrated as a result of core/shell channel architecture.

2:25 p.m.
38.3 Excimer Laser-Annealed Dopant Segregated Schottky (ELA-DSS) Si Nanowire Gate-All-Around (GAA) pFET with Near Zero Effective Schottky Barrier Height (SBH), Y.K. Chin, K.L. Pey*, N. Singh, G.Q. Lo, L.H. Tan, G. Zhu*, X. Zhou*, X.C. Wang**, H.Y. Zheng**, Institute of Microelectronics, *Nanyang Technological University, **Singapore Institute of Manufacturing Technology

We demonstrate excimer laser annealed dopant segregated Schottky (ELA-DSS) silicon nanowire pFETs, achieving an effective Schottky barrier height (SBH) of nearly zero which reduces the parasitic resistance of the fabricated devices and improves the average ON current by 34% as compared to the devices without being treated with laser annealing.

2:50 p.m.
38.4 Integrated Circuits using Top-Gate ZnO Nanowire Transistors with Ultrathin Organic Gate Dielectric, D. Kalblein, H.J. Bottcher, R.T. Weitz, U. Zschieschang, K. Kern*, H. Klauk, Max Planck Institute for Solid State Research, *also with EPFL

We have manufactured top-gate field-effect transistors and circuits based on single crystalline, hydrothermally grown ZnO nanowires with a thin organic gate dielectric. The transistors have large transconductance (1 uS), large on/off ratio (1E7), and steep subthreshold swing (90 mV/decade). Logic circuits with up to four transistors and large gain (35) were realized on a single nanowire.

3:15 p.m.
38.5 Highly Scalable Nonvolatile TiOx/TaSiOy Solid-Electrolyte Crossbar Switch Integrated in Local Interconnect for Low Power Reconfigurable Logic, M. Tada, T. Sakamoto, Y. Tsuji, N. Banno, Y. Saito, Y. Yabe, S. Ishida, M. Terai, S. Kotsuji, N. Iguchi, M. Aono*, H. Hada, N. Kasai, NEC Corporation, *MANA

A fully logic-compatible, nonvolatile crossbar switch using a novel dual-layered TiOx/TaSiOy solid-electrolyte, "NanoBridge" has been developed in a local Cu interconnect layer of a standard CMOS. The cell size is confirmed to be scalable to 50nm keeping the low ON resistance (<100Ω). A key breakthrough is the dual-layered solid-electrolyte, in which TiOx works as an oxygen absorber as well as a superior ionic conductor, thus improving the yield, ON/OFF resistance ratio ($>10^6$) and cycling endurance ($>10^3$).

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