**SHORT COURSE**

**22nm CMOS Technology**

Sunday, December 14, 9:00 a.m. – 5:30 p.m.
Continental Ballrooms 1 - 4

*Course Organizer: Kristin De Meyer, IMEC*

In scaling down CMOS technology towards the 22nm node, the semiconductor community is facing serious challenges. Creativity and innovation will be required in process, device and circuit design. In addition to the standard CV/I speed metric, power and variability are of paramount importance for the 22nm technology node. Among other factors, the power metric is related to the various sources of leakage originating from the gate stack, the high channel doping levels and the poor short channel effects. Controlling these factors requires the use of new materials in front end processes and could possibly lead to the eventual replacement of the planar bulk with device architectures based on ultra thin body SOI, Multi-Gate FET and even alternative channel materials. In that sense the 22nm node might become a real turning point for technology evolution. Variability imposes stringent demands on the new lithography generation and also points in the direction of device designs which are less sensitive to the various sources of variation. Last but not least, the technology choices for the new nodes are starting to have an ever increasing impact on the circuit techniques and methodologies. As a consequence, there is now ever closer interaction between process technology and circuits design, which starts during the early technology definition phase. Examples include lithography driven circuit layout restrictions, circuit impact of process variations and the impact of the back-end technology metrics on circuit density, performance and power.

This course will identify the different roadblocks for 22nm CMOS node and present the solutions being evaluated by the research community to successfully address these roadblocks. In the first talk, the factors involved in technology scaling and the vision of the International Technology Roadmap of Semiconductors (ITRS) will be presented. Various challenges for 22 nm CMOS logic node will be highlighted. The second lecture focuses on the options for performance enhancement in the front end, using mobility boosters, novel gate stacks, series resistance and parasitic capacitance reduction techniques and introduces new device architectures for short channel effect control. In the third lecture the different lithography issues will be discussed including immersion lithography, resolution enhancement techniques, double patterning and EUV lithography. Impact of patterning design rule restrictions on circuit layout will be presented. Challenges for back end processes include the search for new materials to meet high conductivity and low dielectric permittivity, interconnect reliability, electromigration and interaction with assembly and packaging for 3D structures. These issues will be highlighted in the fourth talk. The last lecture will focus on the important issue of device/circuit interactions for the 22nm node and will include discussions on variability, design for manufacturing, device architecture implications of power limitations and the impact of back-end technology elements on overall product performance.

**Introduction**
Instructor*: Kristin De Meyer, IMEC*

**Technology Scaling and Roadmap**
Instructor*: Hiroshi Iwai, Tokyo Institute of Technology*

Introduction
ITRS roadmap
Voltage Scaling
SRAM cell scaling
Low power/Leakage

**22nm Device Architecture and Performance Elements**
Instructor*: Kelin Kuhn, Intel Corporation*

Introduction
    Device scaling challenges
Mobility Enhancement
    Physics of wafer/channel orientation and technology implementation
    Physics of strain (and wafer/channel orientation response)
    Technology approaches to strain (channel/source-drain/external/gate)
    Alternative channel materials
SCE Enhancement
    Physics/technology impact of SCE changes for 22nm
    Conventional enhancement technologies (pocket/abruptness/anneals/etc.)
    Architectural enhancements
        UTB devices
        MUG devices (Trigate, FinFET, other MUG architectures)
Resistance and capacitance enhancement
    Increasing impact of capacitance/resistance effects in 22nm
    Raised S/D technologies
    Advanced silicides
    Metallic source-drain
Advanced Gate Stack Options (HiK/MG)
    Dielectric material (material choices and challenges)
    Workfunction element choices
    Architectural considerations (gate first / gate last / combination)

**Lithography for the 22nm Technology Node**
Instructor: *Kurt Ronse, IMEC*

Introduction
Immersion lithography
    State of the art water based immersion
    Extendibility of immersion with high index materials
Resolution enhancement techniques:
    PSM, Off-Axis, dual exposure, assist features, impact on design rules
Double patterning
    Design split challenges and interaction with design and OPC
    Double patterning process options: Dual exposure versus spacer defined
    Cost-of-ownership
EUV lithography
    EUV critical challenges
    EUV mask challenges
    EUV full field scanner performance

**BEOL Technology for the 22nm Technology Node**
Instructor*: Jeffrey Gambino, IBM*

Integration Options at the 22 nm node: Ultralow-k versus airgap
Metallization options
Advanced CMP Processes
Cu pitch Scaling, Line Resistance
Advanced Packaging/BE interactions
Reliabilty/ Electromigration and TDDB

**Device/Circuit Interactions at the 22 nm Technology Node**
Instructor*: Kaushik Roy, Purdue University*

Device and Circuit Interactions
    Digital and Analog Devices

Impact of possible 22nm node device architectures on circuits

Interconnect Cap and RC issues and product impact

Capacitance & RC scaling trends

Transistor delay vs BE delay trends. Interconnect bottlenecks for 22nm node

22nm node solutions to address reverse RC scaling

Interconnect power delivery issues at 22nm node and technology solutions.

Variations effects at 22nm node

Sources of variations and circuit impact

Solution options in SRAM and logic circuits

Design for Manufacturing Issues

Lithography

Layout and design rules

**Short Course**

**More-than-Moore: Technologies for Functional Diversification**

Sunday, December 14, 9:00 a.m. – 5:30 p.m.
Continental Ballrooms 6 - 9

*Course Organizer: Bin Zhao, Freescale Semiconductor, Irvine, CA*

Over the past 40 years, Moore’s Law has driven the semiconductor industry to continuously improve the performance and capability of microprocessors and memories by relentlessly scaling Si-based CMOS technologies. Along with the exponential rise in computing power and memory capacity, functional diversification enabled by More-than-Moore technologies has also impacted our life beyond the PC: wireless and mobile communication devices, PDA, digital cameras, high-definition displays, entertainment systems, home appliances, automobiles, medical instruments, etc. More-than-Moore technologies, which are beyond the digital CMOS and not necessarily scaled with Moore’s Law, enable formidable implementation and effective integration of non-digital functions, such as power management, analog/RF signal processing, data conversion between analog and digital, sensors and actuators, so as to provide maximum value in diversified functionality, performance, cost, power efficiency, and convenience to use. As CMOS scaling is approaching its fundamental limits, More-than-Moore technologies start to have more profound influence on the semiconductor industry and create new opportunities for growth. This short course reviews the requirements, latest solutions, current challenges and future development of More-than-Moore (MtM) technologies for functional diversification.

The first lecture is focused on power devices and technologies for power management in various applications including automotive, consumer, industrial, and computing. Trends in integration and multifunction of power management ICs are presented with highlights on several key enabling power technologies. The second lecture provides an in-depth review on RF/analog functions and their basic circuit implementations for communications. Key RF and analog circuits are discussed with considerations in circuit design tradeoffs and technology limitations. The third lecture presents CMOS imaging and its related technologies. Advantages, limitations, and future needed breakthroughs in technology and circuit enhancements are reviewed for low cost as well as high performance integrated imaging solutions. The fourth lecture addresses MEMS and heterogeneous integration. The potentials and challenges in modular integration of MEMS with CMOS are discussed along with a review of several successful MEMS products in the marketplace. The final lecture covers the enabling process technologies for functional diversification from an IC foundry perspective, thereby also providing an overview on accessibility of MtM technologies for fabless companies. Manufacturing complexity management and smart qualification process uniquely required by MtM IC products are discussed in detail.

**Introduction and Overview**

*Instructor: Bin Zhao, Freescale Semiconductor*

**Power Devices for Power Management**

*Instructor: Leo Lorenz, Infineon Technologies*

System Requirement for Power Supplies
- Automotive, Consumer, Industrial, Computing

Design Criteria for Power Devices
- High Power Density
- High Efficiency
- DC/DC, DC/AC Converters

Carrier Modulated Power Devices
- IGBT (Insulated Gate Bipolar Transistors)
- FRED (Fast Recovery Epitaxial Diodes), etc

Ultrafast Switching Power Devices
- Super Junction
- LV-MOSFET (<200V)
- SiC

Technology/Application Impacts
- Device Parasitics
- Chip Interfacing and Circuit Setup

Future Development Trends
- Integration
- Multifunction

**RF and Analog IC Design and Implementation**

*Instructor: Thomas Lee, Stanford University*

Overview of Communication Systems

System Considerations
- Dynamic Range
- Noise, Linearity
- Power and Efficiency
- What is Q?
- Tolerance and Parasitics

Representative RF/Analog Building Blocks
- LNA, Mixers, Synthesizers/Oscillators
- Operational Amplifiers
- Power Amplifiers (PA)
- Tuned (Narrowband) vs. Broadband (e.g., UWB) Circuits

Process, Device and Circuit Interactions
- Ft: Its Uses and Abuses
- Scaling Impacts on Matching, Noise, Linearity, Power/Efficiency
- ESD
- PA Lifetime

Design and Implementation
- Modeling Challenges
- Simulation Methodologies

Summary

**CMOS Imaging**

*Instructor: Albert Theuwissen, Delft University of Technology*

Why CMOS Imaging
Fundamentals of CMOS Imaging
  1 T Pixel
  3 T Pixel
  4 T Pixel
  Shared Pixels
Noise Reduction
  Circuit Techniques
  Impact of Semiconductor Technologies
Color Imaging and Signal Processing
  White Balance
  Demosaicing
  Auto-Exposure
  Auto-Focus
Wafer-Level Processing
  Wafer-Level Packaging
  Wafer-Level Optics
  Wafer-Level Camera
Future Perspective

**MEMS on CMOS and Heterogeneous Integration**

*Instructor: Joost van Beek, NXP Semiconductors*

MEMS in Electronic Systems
  Sensors and Actuators: Added Functionality to CMOS
  Electrical Performance Enhancement through MEMS
Physics of Electro-Mechanical Transduction
  Capacitive vs. Inductive
  Piezo-Electric
  Piezo-Resistive
  Thermal Transduction
Integration Approaches
  System-in-Package vs. System-on-Chip Implementation
  Heterogeneous Integration:
  - TSV (through-silicon-vias)
  - Die Stacking
  Modular MEMS on CMOS
  MEMS Packaging
MEMS Solutions
  Consumer: Microphone, Micro-Mirror Array, Accelerometer
  RF MEMS: Switch, BAW, Reference Oscillator
  Others: Gyroscope, Ultrasonic Transducers
MEMS Foundry Process

**IC Foundry Technologies for Functional Diversification**

*Instructor: George Liu, TSMC*

Introduction
MtM Trend in IC Foundry
  Standardization
  Differentiation
MtM Technology Portfolio from IC Foundry

Embedded NVM
Embedded DRAM
Mixed-Mode and RF
High-Voltage and BCD
CMOS Image Sensor
MEMS

MtM Time-to-Market from IC Foundry
Design Platforms
Manufacturing Complexity

**Plenary Session**

Monday, December 15, 9:00 a.m.
Grand Ballroom B

**Welcome and Awards**

General Chair: Ralf Brederlow, Texas Instruments Deutschland GmbH

**Invited Papers**

Technical Program Chair: Vivek Subramanian, University of California, Berkeley

**1.1 Electronic and Ionic Devices: Semiconductor Chips with Brain Tissue**, Peter Fromherz, Max Planck Institute for Biochemistry

The interface between semiconductors and living cells is of great interest to medical science and technology. The realization of signaling and transduction pathways between semiconductor circuits and living tissues will enable dramatic advances in medical prosthetics, biosensorics, brain research and neurocomputation. In this talk, we discuss the electrical interfacing of semiconductors and of living cells, in particular of neurons. Cellular processes are coupled to microelectronic devices through the direct contact of cell membranes and semiconductor chips. The research is directed to reveal the structure and dynamics of the cell-semiconductor interface and to build up hybrid neuroelectronic networks. Thus, we explore the new world at the interface of the electronics in inorganic solids and the ionics in living cells.

**1.2 Non-Volatile Memory Technologies: the Quest for Ever Lower Cost,** Stefan Lai, BeingAMC

Solid-state digital storage has seen a sustained and rapid proliferation over the last few decades. Driven by our insatiable demand for ever more storage, nonvolatile memory technology has been on a path driving towards ever lower cost per bit. In this talk, an overview of the future of nonvolatile memory will be provided. The continued scaling of NAND and NOR Flash memory will be discussed, including a discussion of the scalability challenges therewith. The need for multilevel and multilayer technologies will be analyzed, and various emerging nonvolatile memory technologies will be introduced, driving towards the realization of ultra-dense two-terminal cross point arrays. Process challenges for the realization of future generations of nonvolatile memories will be discussed, as will the role of design and system architecture on the future of nonvolatile memories.

**1.3 PV Technology Trends and Industry's Role**, Tatsuo Saga, Sharp Corporation

The use of photovoltaic technology has increased tremendously over the last decade, driven by substantial cost reductions in photovoltaic modules coupled with increases in conventional energy costs and concerns about the environmental impacts of fossil fuel consumption. In this talk, the future of photovoltaic technology is discussed, including an analysis of technological trends driving the development of next-generation photovoltaic systems. Innovations in silicon photovoltaic panels will be discussed, as will the future of various other types of photovoltaic technologies. The role of the semiconductor industry in

general and the photovoltaic industry in particular on this development will be reviewed, thus providing a comprehensive discussion of the future of this vibrant and proliferating field.

**Session 2: Process Technology - High-k Metal-Gate Integration**
Monday, December 15, 1:30 p.m.
Grand Ballroom A
Co-Chairs: Luigi Colombo, Texas Instruments
Yoshi Tsuchiya, Toshiba America Electronic Components, Inc.

1:30 p.m.
Introduction
1:35 p.m.
**2.1 Intrinsic Correlation Between Mobility Reduction And Vt Shift Due To Interface Dipole Modulation in HfSiON/$SiO_2$ Stack By La Or Al Addition,** K. Tatsumura, T. Ishihara, S. Inumiya, K. Nakajima, A. Kaneko, M. Goto, S. Kawanaka, A. Kinoshita, Toshiba Corporation

Intrinsic Correlation between Mobility reduction and Vt shift due to Interface dipole modulation in HfSiON/$SiO_2$ stack by La or Al addition is clarified. Formation mechanism of dipole governs Vt shift dependence of additional scattering. Al addition increases interface dipole with μ reduction. La addition increases ordered-dipole stack without Î¼ reduction.

2:00 p.m.
**2.2 Intrinsic Origin of Electric Dipoles Formed at High-k/$SiO_2$ Interface,** K. Kita, A. Toriumi, The University of Tokyo

We propose a new model to understand the dipole formation at high-k/Si $O_2$ interface, based on the concept that the areal density difference of oxygen atoms at the interface is the driving force of dipole formation. The validity of our model was partly verified experimentally by using both C-V and XPS measurements.

2:25 p.m.
**2.3 Manipulating Interface Dipoles of Opposing Polarity for Work Function Engineering within a Single Metal Gate Stack,** A.E.-J. Lim, J. Hou, D.-L. Kwong*, Y.-C. Yeo, National University of Singapore, *Institute of Microelectronics

We show that metal gate work function (Φm) pinned by an initial n-type interface dipole can be modulated by forming a p-type interface dipole within the same metal gate stack. We demonstrate the new concept in both TaN/Si $O_2$ and TaN/high-k gate stacks originally pinned by Terbium (Tb) -induced dipole (n-type), through Aluminum (Al) -induced dipole (p-type) formation, after a 950ºC RTA. We show that if n- and p-type dipoles are formed in the same metal gate stack, the net interface dipole polarity will determine the effective gate Φm. In addition, the dominant dipole that results in the metal gate stack hinges critically on the reactions of Al and Tb with $SiO_2$ for Al-O-(Si) and Tb-O-Si bond formation, respectively.

2:50 p.m.
**2.4 Chemical Mechanical Polish: The Enabling Technology (Invited),** J. Steigerwald, Intel Corp.

3:15 p.m.
**2.5 Systematic Study of $V_{th}$ Controllability Using ALD-$Y_2O_3$, $La_2O_3$, and $MgO_2$ Layers with HfSiON/Metal Gate First n-MOSFETs for hp 32 nm Bulk Devices,** S. Kamiyama, D. Ishikawa, E. Kurosawa, H. Nakata, M. Kitajima, M. Ootuka, T. Aoyama, Y. Nara, Y. Ohji, Semiconductor Leading Edge Technologies, Inc.

We present a systematic examination of Vth controllability using $Y_2O_3$, $La_2O_3$, and $MgO_2$ layers by ALD with HfSiON/TaSiN gate first stacks. By employing base- $Y_2O_3$ layers, ultra-thin EOT (0.72nm) can be achieved with excellent Vth controllability (>130mV), high electron carrier mobility, and very high drain current (>1100μA/μm) at 100nA/ μm. Moreover, the PBTI over a 10-year lifetimes can be readily achieved with $V_g$=+1.0V at 125ºC.

3:40 p.m.
**2.6 Device and Reliability Improvement of HfSiON+LaOx/Metal Gate Stacks for 22nm Node Application,** J. Huang, P.D. Kirsch, D. Heh, C.Y. Kang, G. Bersuker, M. Hussain, P. Majhi, P. Sivasubramani, D.C. Gilmer, N. Goel, M.A. Quevedo-Lopez*, C. Young, C.S. Park, C. Park, P. Y. Hung, J. Price, H.R. Harris, B .H. Lee, H.-H. Tseng, R. Jammy, SEMATECH, *University of Texas Dallas

We have demonstrated an advanced gate stack for 22nm LOP application. Troublesome PBTI and mobility degradation issues of low Vt HfSiON+LaOx gate stack are addressed by the optimization of process sequence, LaOx cap thickness and SiON IL. High Ion/Ioff (1250µmA/µm / 100µmA/µm) performance of 0.31 Vt,lin nFETs is achieved without strain booster.

**Session 3 : CMOS Devices and Technology - Advanced Transport Enhancement**
Monday, December 15, 1:30 p.m.
Grand Ballroom B
Co-Chairs: Aaron Thean, Freescale Semiconductor
Tomonari Yamamoto, Fujitsu Laboratories, Ltd.

1:30 p.m.
Introduction
1:35 p.m.
**3.1 High-Performance nMOSFET With In-Situ Phosphorus-Doped Embedded Si:C (ISPD eSi:C) Source-Drain Stressor,** B. Yang, R. Takalkar*, Z. Ren*, L. Black, A. Dube*, J.W. Weijtmans, J. Li*, J.B. Johnson*, J. Faltermeier^, A. Madan*, Z. Zhu*, A. Turansky*, G. Xia*, A. Chakravarti*, R. Pal, K. Chan^, A. Reznicek^, T.N. Adam^, B. Yang, J.P. de Souza^, E.C.T. Harley*, B. Greene*, A. Gehring, M. Cai*, D. Aime[#], S. Sun*, H. Meer, J. Holt, D. Theodore[#], S. Zollner[#], P. Grudowski[#], D. Sadana^, D.-G. Park^, D. Mocuta*, D. Schepis*, E. Maciejewski*, S. Luning, J. Pellerin, E. Leobandung*, Advanced Micro Devices, *IBM Microelectronics, ^IBM T.J.Watson Research Center, [#]Freescale Semiconductor, Inc.

This paper reports for the first time that eSi:C is a superior nMOSFET stressor compared to the combination of SMT and tensile stress liner. nMOSFET channel mobility and drive current were significantly enhanced by eSi:C compared to our best high-performance 45nm-node-baseline employing SMT and tensile liner stressors.

2:00 p.m.
**3.2 Physical and Electrical Analysis of the Stress Memorization Technique (SMT) using Poly-gates and its Optimization for Beyond 45 nm High Performance Applications,** T. Miyashita, T. Owada*, A. Hatada*, Y. Hayami, K. Ookoshi*, T. Mori*, H. Kurata, T. Futatsugi, Fujitsu Laboratories, Ltd., *Fujitsu Microelectronics Limited

We have investigated the stress memorization technique (SMT) using poly-gates through both physical analysis and electrical characteristics. By optimizing key factors in the SMT proces with As-NSD, we have achieved highly enhanced NFET performance with high scalability for beyond 45nm high performance applications.

2:25 p.m.
**3.3 (110) NMOSFETs Competitive to (001) NMOSFETs: Si Migration to Create (331) Facet and Ultra-Shallow Al Implantation after NiSi Formation,** H. Fukutome, K. Okabe*, K. Okubo, H. Minakata, Y. Morisaki, K. Ikeda, T. Yamamoto, K. Hosaka, Y. Momiyama, M. Kase, S. Satoh, Fujitsu Laboratories Ltd., *Fujitsu Microelectronics Limited

We demonstrated for the first time device performance of (110) nMOSFETs featuring Si migration process (better mobility and modified shape of narrow active) and ultra-shallow Al implantation after NiSi formation (reduced parasitic resistance). (110) nMOSFETs became competitive to (001) nMOSFETs with keeping advantage of 40% in (110) pMOSFET performance.

2:50 p.m.
**3.4 High Performance Hi-K + Metal Gate Strain Enhanced Transistors on (110) Silicon,** P. Packan, S. Cea, H. Deshpande, T. Ghani, M. Giles, O. Golonzka, M. Hattendorf, R. Kotlyar, K. Kuhn, A. Murthy, P. Ranade, L. Shifren, C. Weber, K. Zawadzki, Intel Corporation

The performance impact of (110) silicon substrates on high-k + metal gate strained 45nm node devices are presented. Record PMOS drive currents of 1.2 ma/um at 1.0V at 100nA/um Ioff are reported. 2D short channel effects are shown to mitigate the negative impact of (100) substrates on NMOS performance.

3:15 p.m.
**3.5 Experimental Investigation on the Origin of Direction Dependence of Si (110) Hole Mobility Utilizing Ultra-Thin Body pMOSFETs,** K. Shimizu, T. Saraya, T. Hiramoto, University of Tokyo

The direction dependence of hole mobility in (110) SOI pFETs has been systematically investigated for the first time utilizing a new device structure. It is newly found that the high hole mobility in Si (110)/<110> even at high electric field originates from both the large subband energy difference and conductivity mass change caused by quantum confinement.

**Session 4: Displays, Sensors and MEMS - Thin-Film Devices and Memory**
Monday, December 15, 1:30 p.m.
Continental Ballroom 1 – 3
Co-Chairs: Matsuko Hatano, Hitachi Ltd.
David Redinger, 3M Company

1:30 p.m.
Introduction
1:35 p.m.
**4.1 High Performance Oxide Thin Film Transistors with Double Active Layers,** S.I. Kim, C.J. Kim, J.C. Park, I. Song, S.W. Kim, H. Yin, E. Lee, J.C. Lee, Y. Park, Samsung Advanced Institute of Technology

We successfully integrated the high performance oxide thin film transistors with double active layers. The active layer is composed of IZO (or ITO) and GIZO layers. The TFT shows a high mobility of $104cm^2/V.sec$, the acceptable threshold voltage of about 0.5V and the low $V_{th}$ shift less than 1V under voltage stress. These are very promising results for applications in driving large area AMOLED and AMLCD display.

2:00 p.m.
**4.2 1.5-V Operating Fully-Depleted Amorphous Oxide Thin Film Transistors Achieved by 63-mV/dec Subthreshold Slope,** T. Kawamura, H. Uchiyama, S. Saito, H. Wakana, T. Mine, M. Hatano, K. Torii, T. Onai, Hitachi Ltd.

Amorphous InGaZnO TFTs achieving 63-mV/dec subthreshold slope were demonstrated. To achieve the small subthreshold slope as well as small $I_{off}$, fully-depleted off-state was employed by thinning the channel layer to 6 nm. For Vg = 0 to 1.5 V operation, $I_{off} < 10^{-17}$ A/µm, on/off ratio $> 10^8$ were obtained.

2:25 p.m.
**4.3 Bootstrapped Ring Oscillator with Propagation Delay Time below 1.0 nsec/stage by Standard 0.5µm Bottom-Gate Amorphous $Ga_2O_3$-$In_2O_3$-ZnO TFT Technology,** H. Yin, S. Kim, C.J. Kim, J. Park, I. Song, S.-W. Kim, S.-H. Lee, Y. Park, Samsung Advanced Institute of Technology

The novel 3TFTs bootstrapped ring oscillator with the standard 0.5um bottom-gate amorphous $Ga_2O_3$-$In_2O_3$-ZnO TFT technology after some parameters optimization is reported. The propagation delay time of 0.94 ns/stage for a supply voltage of 9V is achieved in the 5-stage ring oscillator, which is over 75 times faster than the previous report.

2:50 p.m.
**4.4 Stack Friendly All-Oxide 3D RRAM using GaInZnO Peripheral TFT Realized over Glass Substrates,** M.-J. Lee, C.B. Lee, S. Kim, H. Yin, J. Park, S.E. Ahn, B.S. Kang, K.H. Kim, G. Stefanovich, I. Song, S.-W. Kim, J.H. Lee, S.J. Chung, Y.H. Kim, C.S. Lee, J.B. Park, I.G. Baek*, C.J. Kim, Y. Park, Samsung Advanced Institute of Technology, *Samsung Electronics Co. Ltd.

This paper reports on new concept consisting of all-oxide-based device component for future high density non-volatile data storage with stackable structure. We demonstrate that using of all-oxide-based device components: a GaInZnO (GIZO) thin film transistors (TFTs) integrated with 1D (CuO/InZnO)-1R (NiO) (one diode-one resistor) structure oxide memory node element, provide necessary conditions. Also, we herein propose a new concept of stacked-memory structure to minimize on-chip real estate to maximize integrated density.

3:15 p.m.
**4.5 Amorphous Silicon Thin-Film Transistors with DC Saturation Current Half-Life of More than 100 Years,** B. Hekmatshoar, K.H. Cherenack, S. Wagner, J.C. Sturm, Princeton University

We report amorphous silicon TFT's with a saturation current half-life of more than 100 years, an improvement of above 1000X compared to previous art. This half-life is 10X higher than the half-life of high quality green OLED's showing that the TFT's are promising for driving OLED's in active-matrix OLED displays.

3:40 p.m.
**4.6 Ultra-High Frequency Rectification Using Organic Diodes,** S. Steudel, K. Myny, P. Vicca, D. Cheyns, J. Genoe, P. Heremans, IMEC

Research towards organic RFID tags is one of the main drivers of the field of organic electronics, because low-cost plastic RFID tags could replace barcodes in the future. In this work, we show for the first time that a plastic diode can even operate in the Ultra-High Frequency band (433MHz, 869MHz, 915MHz).

4:05 p.m.
**4.7 A Large-Area, Flexible, Ultrasonic Imaging System With A Printed Organic Transistor Active Matrix,** Y. Kato, T. Sekitani, Y. Noguchi, M. Takamiya, T. Sakurai, T. Someya, The University of Tokyo

We have successfully fabricated a large-area, flexible, ultrasonic system by integrating a two-dimensional polymeric ultrasonic transducer array with a printed organic transistor active matrix. The new sheet-type device can offer a cost-effective solution for a real-time three-dimensional imaging in free space and/or a large-area proximity sensor for robot skins.

**Session 5: Characterization, Reliability, and Yield - BTI in SiON and High k FETs**
Monday, December 15, 1:30 p.m.
Continental Ballroom 4
Co-Chairs: Sufi Zafar, IBM T.J. Watson Research Center
Gennadi Bersuker, Sematech

1:30 p.m.
Introduction
1:35 p.m.
**5.1 A Comprehensive Study of Flicker Noise in Plasma Nitrided SiON p-MOSFETs: Process Dependence of Pre-Existing and NBTI Stress Generated Trap Distribution Profiles,** G. Kapila, N. Goyal, V.D. Maheta, C. Olsen*, K. Ahmed*, S. Mahapatra, IIT Bombay, *Applied Materials

Slope and magnitude of flicker noise before and after NBTI stress is studied. Noise slope is identified as a sensitive monitor of trap distribution in SiON bulk. A direct correlation of pre-stress traps to N distribution

is established. Post-stress traps are shown to generate close to the Si/SiON interface. Noise magnitude (pre-stress) strongly correlates with atomic N density (N%), and shows identical field acceleration (post-stress) as charge pumping (CP) and drain current (I-V) measurements.

2:00 p.m.
**5.2 Universality of Interface Trap Generation in Strained/Unstrained PMOS Devices During NBTI Stress,** A.E. Islam, J.H. Lee*, W.H. Wu*, A. Oates*, M.A. Alam, Purdue University, *Taiwan Semiconductor Manufacturing Corporation

Despite extensive use of strained technology in CMOS, it is still unclear whether NBTI-induced NIT-generation in strained devices is different from unstrained devices. Here, we present a universal picture for NIT-generation in strained/unstrained devices and show appropriately designed strained devices might reduce NBTI being a concern for CMOS scaling.

2:25 p.m.
**5.3 A Comprehensive and Comparative Study of Interface and Bulk Characteristics of nMOSETs with La-Incorporated High-*k* Dielectrics,** W.-H. Choi, H.-M. Kwon*, I.-S. Han*, T.-G. Goo*, M.-K. Na*, C.Y. Kang, B.H. Lee, H.-D. Lee, R. Jammy, SEMATECH, *Chungnam National University

For the first time, device performance and reliability of La incorporated high-k dielectrics, HfLaSiON and HfLaON, are comprehensively and comparatively characterized. It is revelaed that HfLaSiON has a strong relationship with the interface characteristics and barrier height, while HfLaON with the bulk trap characteristics.

2:50 p.m.
**5.4 The Impact of La-Doping on the Reliability of Low $V_{th}$ High-k/Metal Gate nMOSFETs Under Various Gate Stress Conditions,** C.Y. Kang, C.D. Young, J. Huang, P. Kirsch, D. Heh, P. Sivasubramani, H.K. Park, G. Bersuker, B.H. Lee, H.S. Choi*, K.T. Lee*, Y-H. Jeong*, J. Lichtenwalner^, A.I. Kingon^, H-H Tseng, R. Jammy, SEMATECH, *POSTECH, ^North Carolina State University

We report results of comprehensive reliability study for La-doped HfSiO dielectrics using PBTI, TDDB and flicker noise. Due to La-induced interface dipole formation and La-incorporation, the La-doped high-k devices exhibit different reliability behavior depending on gate stress field. With process optimization, we demonstrate that this reliability issues can be minimized while maintaining good device characteristics.

3:15 p.m.
**5.5 Physical Model of the PBTI and TDDB of La Incorporated HfSiON Gate Dielectrics with Pre-existing and Stress-Induced Defects,** M. Sato, N. Umezawa*, J. Shimokawa, H. Arimura**, S. Sugino^, A. Tachibana^, M. Nakamura, N. Mise, S. Kamiyama, T. Morooka, T. Eimori, K. Shiraishi^^, K. Yamabe^^, H. Watanabe**, K.Yamada#, T. Aoyama, T. Nabatame, Y. Nara, Y. Ohji, Selete, *NIMS, **Osaka University, ^Kyoto University, ^^University of Tsukuba, #Waseda University

We have clarified the impact on reliability of La incorporation into the HfSION gate dielectrics nMOSFETs (PBTI, TDDB). Although La incorporation is effective on pre-existing defects suppression, stress induced defect generation is more sensitive to stress voltage and temperature. This is caused by the elevating the energy level of oxygen vacancy and high ionicity of La-O bond.

3:40 p.m.
**5.6 Impacts of Non-negligible Electron Trapping/Detrapping on the NBTI Characteristics in Silicon Nanowire Transistors with TiN Metal Gates,** L. Zhang, R. Wang, J. Zhuge, R. Huang, D.-W. Kim*, D. Park*, Y. Wang, Peking University, *Samsung Electronics Co.

Impacts of electron trapping/detrapping on the NBTI in silicon nanowire transistors (SNWTs) with metal gates are experimentally studied. Both stress and recovery characteristics of NBTI in SNWTs are severely impacted by the electron trapping/detrapping behavior. The generation of new-born trap-precursors was also observed and discussed, which can lead to additional unexpected reliability degradation of SNWTs.

**Session 6: Quantum, Power, and Compound Semiconductors Devices - High-Voltage Power Devices**
Monday, December 15, 1:30 p.m.
Continental Ballroom 5
Co-Chairs: Tomas Palacios, Massachusetts Institute of Technology
Florin Udrea, Cambridge University

1:30 p.m.
Introduction
1:35 p.m.
**6.1 Rugged Dotted-Channel LDMOS Structure,** T. Khan, V. Khemka, R. Zhu, A. Bose, Freescale Semiconductor

A unique dotted channel structure for improved robustness is presented to enhance the operating envelope for LDMOS devices. The proposed device aims to break the age-old conundrum of the trade-off triangle between BVDSS-Rds, on-SOA where improvement in one results in severe penalty for the other.

2:00 p.m.
**6.2 190V N-Channel Lateral IGBT Integration in SOI 0.35µm BCD Technology,** M. Sambi, M. Gallo, P. Galbiati, STMicroelectronics

The Integration of 190V N-Ch. LIGBT in SOI 0.35µm shrunk BCD technology is here described. LIGBT was simulated and characterized, both to exploit electrical performances and HTRB behavior. The novel device shows a very high saturation current (around 2.5kA $cm^2$) and good HTRB robustness

2:25 p.m.
**6.3 High Voltage Devices Integration Into Advanced CMOS Technologies (Invited),** R.A. Bianchi, F. Monsieur, F. Blanchet, C. Raynaud, O. Noblanc, STMicroelectronics TRD

This paper focuses on CMOS technologies for mobile applications having integrated high voltage devices to address analog baseband and RF power applications. Technology evolution and some selected device architectures are reviewed. Main challenges encountered when integrating these devices in advanced CMOS are explained. New results and some considerations on performance-reliability trade-off are provided.

2:50 p.m.
**6.4 Monolithic Integration of Lateral Field-Effect Rectifier with Normally-off HEMT for GaN-on-Si Switch-mode Power Supply Converters,** W. Chen, K.-Y. Wong, K.J. Chen, Hong Kong University of Science and Technology

High-performance lateral field-effect rectifiers and normally-off HEMTs are successfully integrated using conventional GaN-on-Si wafers. The rectifier features a 470 V breakdown voltage and a 2.04 mΩ $cm^2$ on-resistance. A boost converter that features a single active device chip is demonstrated for proof-of-concept of GaN-based integrated switch-mode power supply.

3:15 p.m.
**6.5 GaN-based Natural Super Junction Diodes,** H. Ishida, D. Shibata, H. Matsuo, M. Yanagihara, Y. Uemoto, T. Ueda, T. Tanaka, D. Ueda, Matsushita Electric Industrial Co., Ltd.

We propose a new breakdown mechanism of GaN-based electron devices called "Natural Super Junction". The junction model is confirmed by device simulations and experimental results for newly developed multi-channel diodes, which realize reducing the on-resistance to 176 mΩ $cm^2$ with keeping extremely breakdown voltage of 9300V.

3:40 p.m.

**6.6 Source Injection Induced Off-State Breakdown and Its Improvement by Enhanced Back Barrier with Fluorine Ion Implantation in AlGaN/GaN HEMTs,** M. Wang, K.J. Chen, Hong Kong University of Science and Technology

AlGaN/GaN HEMTs off-state breakdown is investigated and it is found that source-injection through the buffer with the following impact ionization is the dominant three-terminal off-state breakdown mechanism. A 35% improvement of the breakdown voltage could be achieved in enhanced back barrier HEMT by implanting fluorine ions under the channel region.

**Session 7: Solid State and Nanoelectronic Devices - Spin Devices, Batteries and Steep Slope FETs**
Monday, December 15, 1:30 p.m.
Continental Ballroom 6
Co-Chairs: Franz Kreupl, Qimonda AG
Jing Guo, University of Florida

1:30 p.m.
Introduction
1:35 p.m.
**7.1 Engineering Single Spins And Coherence For Spintronics (Invited),** D.D. Awschalom, University of California Santa Barbara

c-V measurements under light illumination and under wide range of temperatures have been performed on UHV- deposited $Al_2O_3$(3nm)/$Ga_2O_3$($Gd_2O_3$)(8.5nm) on n- and p-$In_{0.2}Ga_{0.8}As$/GaAs. The results exhibit very high-quality interface and free-moving Fermi-level.

2:00 p.m.
**7.2 Magnetic Coupled Spin-Torque Devices and Magnetic Ring Oscillator,** L. Leem, J.S. Harris, Stanford University

Magnetic Coupled Spin-torque Device (MCSTD) is a new spintronics device architecture that circumvents difficulties in spin transfer and spin detection by applying spin torque transfer technique and magnetic coupling induced asymmetric energy barriers. Device gain, device switching speed, inversion capability and new interconnect techniques of MCSTD are presented. Three stage MCSTD ring oscillator is demonstrated in micromagnetics simulations.

2:25 p.m.
**7.3 Impact of SOI, $Si_{1-x}Ge_x$OI and GeOI Substrates on CMOS Compatible Tunnel FET Performance,** F. Mayer, C. Le Royer, J.-F. Damlencourt, K. Romanjek, F. Andrieu, C. Tabone, B. Previtali, S. Deleonibus, CEA-LETI

We report for the first time experimental investigations on SOI, $Si_{1-x}Ge_x$OI & GeOI Tunnel FET (TFET) and successfully solve the TFET bipolar parasitic conduction by a novel TFET architecture, the Drift Tunnel FET (DTFET), with improved OFF state control. Moreover, we demonstrate for the first time functional TFET & CMOS devices on $Si_{1-x}Ge_x$OI (x=15-30-100%) co-integrated with the same SOI process flow, enabling TFET $I_{ON}$ continuous improvement with Ge content increase: $I_{ON}$ x2700 for GeOI (compared to SOI).

2:50 p.m.
**7.4 Demonstration of Subthrehold Swing Smaller Than 60mV/decade in Fe-FET with P(VDF-TrFE)/$SiO_2$ Gate Stack,** G.A. Salvatore, D. Bouvet, A.M. Ionescu, Ecole Polytechnique Federale de Lausanne

We experimentally show, for the first time that by integrating a thin ferroelectric layer into a gate stack of a standard MOS transistor one can overcome the 60mV/decade physical limit of the subthreshold swing. We demonstrate sub-threshold swings as low as 13mV/dec at room temperature and explain them by the negative capacitance of the ferroelectric layer at low fields.

3:15 p.m.
**7.5 Feedback FET: A Novel Transistor Exhibiting Steep Switching Behavior at Low Bias Voltages,** A. Padilla, C.W. Yeung, C. Shin, M.H. Cho, C. Hu, T.-J. King Liu, University of California Berkley

A novel transistor design which utilizes positive feedback to achieve steep switching behavior upon the onset of impact ionization in the high-field drain-offset region is proposed and demonstrated. The FB-FET exhibits very low SS (<10 mV/dec at room temperature) and very high $I_{ON}/I_{OFF}$ ratio (~$10^8$) for relatively low operating voltages (<1V), and can be operated as an n-channel device or p-channel device, and potentially as a NVM cell. It is a candidate for future low-power electronic devices.

3:40 p.m.
**7.6 Nanowire Batteries for Next Generation of Electronics (Invited),** C.K. Chan, S.T. Connor, C.-M. Hsu, R.-A. Huggins, Y. Cui, Stanford University

**Session 8: Modeling and Simulation - Advances in Modeling Low Dimensional Structures**
Monday, December 15, 1:30 p.m.
Continental Ballroom 7 – 9
Co-Chairs: Giuseppe Iannaccone, Università di Pisa
Pierpaolo Palestri, University of Udine

1:30 p.m.
Introduction
1:35 p.m.
**8.1 From NEMO1D And NEMO3D To OMEN: Moving Towards Atomistic 3-D Quantum Transport In Nano-Scale Semiconductors (Invited),** G. Klimeck, M. Luisier, Purdue University

Lessons learned in 15 years of NEMO development starting from quantitative and predictive resonant tunneling diode (RTD) to multi-million atom electronic structure modeling and the path for One More Embodiment of NEMO (OMEN) are laid out. The recent OMEN capabilities enable realistically large 3D atomistic nano-scale device simulation.

2:00 p.m.
**8.2 Shot Noise In Quasi-One Dimensional FETs,** A. Betti, G. Fiori, G. Iannaccone, Università di Pisa

The noise of the drain current of ballistic Carbon Nanotube and Silicon Nanowire FETs is essentially shot noise. The combined effect of Pauli exclusion and Coulomb repulsion suppresses noise down to 27% of full shot noise. Results are obtained from NEGF simulations of random electron injection from the contacts.

2:25 p.m.
**8.3 Impact of Strain on the Performance of Ge-Si Core-Shell Nanowire Field Effect Transistors,** Y. He, Y. Zhao, S. Yu, C. Fan, G. Du, J. Kang, R. Han, X. Liu, Peking University

A new simulation method is developed to evaluate strain effect on Ge-Si core-shell NW p-FET performance from band structures to hole transport both in ballistic transport and in phonon scattering cases. Simulation results indicate that thicker shell will enhance transistor performance substantially.

2:50 p.m.
**8.4 The Quantum Capacitance Limit of High-Speed, Low-Power InSb Nanowire Field Effect Transistors,** M.A. Khayer, R.K. Lake, University of California Riverdale

The diameter dependent performance metrics of InSb NWFETs operating in the quantum capacitance limit is theoretically investigated for the first time. Both energy-delay and power-delay products are minimized

by choosing NW diameters of 10-40 nm with Efs of 0.1 eV. These NWFETs provide both ultra low-power switching and high speed.

3:15 p.m.
**8.5 Modeling of Schottky and Ohmic Contacts between Metal and Graphene Nanoribbons using Extended Hückel Theory-Based NEGF Method,** X. Guan, Q. Ran*, M. Zhang*, Z. Yu, H.-S.P. Wong, Stanford University, *Tsinghua University

Atomistic quantum transport simulation is performed on Schottky and ohmic metal-GNR contacts with different metal electrodes. Effects induced by changing the GNR orientation or layer numbers are discussed. The interface dipole due to the polarization of chemical bond is found to have a significant impact on the contact behavior.

3:40 p.m.
**8.6 Graphene Nano-Ribbon (GNR) Interconnects: A Genuine Contender or a Delusive Dream?,** C. Xu, H. Li, K. Banerjee, University of California Santa Barbara

A comprehensive conductance and delay analysis of graphene nano-ribbon (GNR) interconnects is presented. Several GNR structures and other interconnect materials are compared. Till the very end of ITRS roadmap, GNRs cannot match the performance of Cu or SWCNTs, unless proper intercalation doping is used and specular nano-ribbon edge is achieved.

**Session 9: Memory Technology - Phase-Change and Unified Memory**
Monday, December 15, 1:30 p.m.
Imperial Ballroom
Co-Chairs: Daniele Ielmini, Politecnico di Milano
Gitae Jeong, Samsung Electronics Co., Ltd.

1:30 p.m.
Introduction
1:35 p.m.
**9.1 Mechanisms of Retention Loss in $Ge_2Sb_2Te_5$-based Phase-Change Memory,** Y.H. Shih, J.Y. Wu, B. Rajendran*, M.H. Lee, R. Cheek*, M. Lamorey**, M. Breitwisch*, Y. Zhu*, E.K. Lai, C.F. Chen, E. Stinzianni*, A. Schrott*, E. Joseph*, R. Dasaka*, S. Raoux^, H.L. Lung, C. Lam*, Macronix International, *IBM TJ Watson Research Center, **IBM, ^IBM Almaden Research Center

Data retention loss from the amorphous (RESET) state over time in Phase-Change Memory cells is associated with spontaneous crystallization. Two fundamental mechanisms that affect the retention loss behavior are identified. The results suggest that (i) an optimized RESET operation produces a fully amorphized $Ge_2Sb_2Te_5$ (aGST) active region, with no crystalline domains inside, (ii) cells in the tail distribution fail to retain their amorphous (RESET) state due to spontaneous generation of crystallization nuclei and grain growth, and (iii) cells in the normal distribution fail due to grain growth from the amorphous/crystalline GST boundary, instead of nucleation within the active region.

2:00 p.m.
**9.2 A Unified 7.5nm Dash-Type Confined Cell for High Performance PRAM Device,** D.H. Im, J.I. Lee, S.L. Cho, H.G. An, D.H. Kim, H. Park, D.H. Ahn, H. Horii, S.O. Park, U.-I. Chung, J.T. Moon, and W.S. Lee, Samsung Electronics Co. Ltd.

We present a new-type confine structure within 7.5nm width dash contact for sub 20nm generation PRAMs. Phase Change Material by CVD was perfectly filled in a dash contact without void. The reset current is ~160μA and the programming speed is 50 ns with a high reliability.

2:25 p.m.
**9.3 Transient Effects Of Delay, Switching And Recovery In Phase Change Memory (PCM) Devices,** S. Lavizzari, D. Ielmini, D. Sharma, A.L. Lacaita, Politecnico di Milano

A comprehensive characterization and physical modeling of PCM transient effects, namely delay, switching and recovery times is presented; allowing for the first time to calculate the statistical impact of read disturb and the ultimate speed limitations to set, reset and program/verify loop times.

2:50 p.m.
**9.4 Characterization and Modeling of Low-Frequency Noise in PCM Devices,** P. Fantini, G. Betti Beneventi*, A. Calderoni, L. Larcher*, P. Pavan*, F. Pellizzer, Numonyx, R&D, *Università delgi Studi di Modena e Reggio Emilia

GST-based Phase Change Memories (PCM) are among the privileged candidate for the next Non-Volatile Memory (NVM) technology generation. Low-frequency noise attracted very attention in the engineering of NVM technologies definition with nanoscale sizes. In this work, we investigate the low-frequency noise in PCM devices providing a new physical model for the amorphous GST ($Ge_2Sb_2Te_5$) material. Noise intensity is characterized and modeled as a function of bias, temperature and size. Findings from 1/f noise analysis are used to understand the drift mechanism of the amorphous state resistance.

3:15 p.m.
**9.5 High Speed Flash Memory and 1T-DRAM on Dopant Segregated Schottky Barrier (DSSB) FinFET SONOS for Multi-functional SoC Applications,** S.-J. Choi, J.-W. Han, S. Kim, D.-H. Kim, M.-G. Jang*, J.-H. Yang*, J.S. Kim**, K.H. Kim**, G.S. Lee**, J.S. Oh**, M.H. Song**, Y.C. Park**, J.W. Kim**, Y.-K. Choi, KAIST, *ETRI, **National Nanofab Center

A novel Dopant-Segregated Schottky-Barrier (DSSB) FinFET SONOS is demonstrated for multi-functioning with high-speed NVM and 1T-DRAM. Hot electrons energized by energy band bending at DSSB were used for fast program, which results in 3.5V of Vth shift for program time of 100ns. 1T-DRAM is also demonstrated in the same device.

3:40 p.m.
**9.6 Energy Band Engineered Unified-RAM (URAM) for Multi-Functioning 1T-DRAM and NVM,** J.-W. Han, S.-W. Ryu, S. Kim, C.-J. Kim, J.-H. Ahn, S.-J. Choi, K.J. Choi*, B.J. Cho, J.S. Kim**, K.H. Kim**, G.S. Lee**, J.S. Oh**, M.H. Song**, Y.C. Park**, J.W. Kim**, Y.-K. Choi, KAIST, *Jusung Engineering, **National Nanofab Center

An energy band engineered unified-RAM (URAM) is demonstrated in hetero-epitaxially grown $Si/Si_{1-x}Ge_x$ substrates. The combination of O/N/O and the floating body provides non-volatile memory and capacitorless 1T-DRAM function in a single transistor. The URAM provides memory design flexibility for embedded memory applications.

**Session 10: CMOS Devices and Technology - Vth Variation and Scaling**
Tuesday, December 16, 9:00 a.m.
Grand Ballroom A
Co-Chairs: Olivier Faynot, CEA Grenoble
Eddie Breashears, Texas Instruments

9:00 a.m.
Introduction
9:05 a.m.
**10.1 Scaling of 32nm Low Power SRAM with High-K Metal Gate,** H.S. Yang, R. Wong, R. Hasumi[1], Y. Gao[2], N.S. Kim[2], D.H. Lee[3], S. Badrudduza[4], D. Nair, M. Ostermayr[5], H. Kang[3], H. Zhuang[5], J. Li, L. Kang[4], X. Chen, A. Thean[4], F. Arnaud[5], L. Zhuang, C. Schiller, D.P. Sun[2], Y.W.Teh[2], J. Wallner, Y. Takasu[1], K. Stein, S. Samavedam[4], D. Jaeger, C.V. Baiocco, M. Sherony, M. Khare, C. Lage[4], J. Pape, J. Sudijono[2], A.L. Steegen, S. Stiffler, IBM Microelectronics SRDC, [1]Toshiba, [2]Chartered Semiconductor, [3]Samsung Electronics, [4]Freescale Semiconductor, [5]Infineon Technologies, [6]STMicroelectronics

This paper describes SRAM scaling for 32nm low power bulk technology, enabled by high-K metal gate process, down to 0.149μm$^2$ and 0.124 μm$^2$. SRAM access stability and write margin are significantly improved through a 50% Vt mismatch reduction, thanks to HK-MG $T_{inv}$ scaling. Cell read current is increased by 70% over Poly-SiON process. Ultra dense cell process window is expanded with optimized contact process. A dual-ground write assist option can additionally enable ultra dense 0.124 μm$^2$ cell to meet low power application requirements.

9:30 a.m.
**10.2 Demonstration of Highly Scaled FinFET SRAM Cells with High-*k* /Metal Gate and Investigation of Characteristic Variability for the 32 nm Node and Beyond,** H. Kawasaki*, M. Khater, M. Guillorn, N. Fuller, J. Chang, S. Kanakasabapathy, L. Chang, R. Muralidhar**, K. Babich, Q. Yang, J. Ott, D. Klaus, E. Kratschmer, E. Sikorski, R. Miller^,Y. Zhang, J. Silverman, C. Ouyang, A. Yagishita*, M. Takayanagi*, W. Haensch, K. Ishimaru*, *Toshiba America Electronic Components Inc., IBM TJ Watson Research Center , **Freescale Semiconductor, ^Advanced Micro Devices

Highly scaled FinFET SRAM cells, of area down to 0.128 μm$^2$, were fabricated using HKMG to investigate characteristic variability. A single-sided I/I scheme was proposed to reduce $V_t$. In the 0.187 μm$^2$ cell, at Vd = 0.6 V, a SNM of 95 mV was obtained and stable read/write operations were verified.

9:55 a.m.
**10.3 First Observation Of Finfet Specific Mismatch Behavior And Optimization Guidelines For SRAM Scaling,** T. Merelle, G. Curatola, A. Nackaerts, N. Collaert*, M.J.H. van Dal, G. Doornbos, T.S. Doorn**, P. Christie, G. Vellianitis, B. Duriez, R. Duffy, B.J. Pawlak, F.C. Voogt**, R. Rooyackers*, L. Witters*, M. Jurczak*, R.J.P. Lander, NXP-TSMC Research Center, *IMEC, **NXP Semiconductors

$V_t$-mismatch, and thus SRAM scalability, is greatly improved in narrow SOI FinFETs, with respect to planar bulk, because of their undoped channel and near-ideal gate control. Simulations and measurements show that in FinFETs, β-mismatch becomes dominant, leading to radically different SRAM characteristics. Careful process tuning induces a substantial reduction in β-mismatch. Impact of this novel mismatch behavior on SRAM is demonstrated. This study provides guidelines for SRAM design in a FinFET technology.

10:20 a.m.
**10.4 High Immunity to Threshold Voltage Variability in Undoped Ultra-Thin FDSOI MOSFETs and its Physical Understanding,** O. Weber, O. Faynot, F. Andrieu, C. Buj-Dufournet, F. Allain, P. Scheiblin, J. Foucher, N. Daval*, D. Lafond, L. Tosti, L. Brevard, O. Rozeau, C. Fenouillet-Beranger, M. Marin**, F. Boeuf**, D. Delprat*, K. Bourdelle*, B.-Y. Nguyen*, S. Deleonibus, CEA-LETI MINATEC, *SOITEC, **STMicroelectronics

Sources responsible for local and inter-die threshold voltage (Vt) variability in undoped ultra-thin FDSOI MOSFETs with a high-k/metal gate stack are experimentally discriminated for the first time. Charges in the gate dielectric and/or TiN gate workfunction fluctuations are determined as major contributors to the local Vt variability and it is found that SOI thickness (TSi) variations have a negligible impact down to TSi=7nm. Moreover, TSi scaling is shown to limit the Vt variability induced by gate length fluctuations.The highest matching performance ever reported for 25nm gate length MOSFETs is achieved ($A_{Vt}$=0.95mV.μm), demonstrating the effectiveness of the undoped ultra-thin FDSOI architecture in terms of Vt variability control.

10:45 a.m.
**10.5 Comprehensive Study on $V_{th}$ Variability in Silicon on Thin BOX (SOTB) CMOS with Small Random-Dopant Fluctuation: Finding a Way to Further Reduce Variation,** N. Sugii, R. Tsuchiya, T. Ishigaki, Y. Morita, H. Yoshimoto, K. Torii, S. Kimura, Hitachi Ltd.

SOTB has the smallest Vth variation among planar CMOS due to low-dose channel. Short-channel-effect immunity and body-thickness uniformity is the key to further reducing the variation. An often mentioned

phenomenon, larger variability in NMOS than PMOS, cannot be explained by conventional RDF but is surely related to channel doping.

11:10 a.m.
**10.6 MOSFET Performance Scaling: Limitations and Future Options (Invited),** D.A. Antoniadis, A. Khakifirooz, Massachusetts Institute of Technology

Prospects of velocity enhancement as the main driver of the performance scaling in future CMOS is examined. Limits of velocity enhancement in uniaxially strained Si are first presented and then outlooks of novel channel materials such as Ge and III-V semiconductors are discussed. Finally, characteristics of performance scaling under power dissipation constraints are studied.

11:35 p.m.
**10.7 Improved Effective Switching Current ($IEFF^+$) and Capacitance Methodology for CMOS Circuit Performance Prediction and Model-to-Hardware Correlation,** X. Yu, S.-J. Han, N. Zamdmer, J. Deng, E.J. Nowak, K. Rim, IBM SRDC

Two separate IEFF definitions are adopted for delay performance prediction (IEFF ), and ring AC/DC prediction-to-hardware correlation analysis (IEFF+). IEFF+ captures linear current effect and results in perfect matching in ring AC and DC effective resistance across SOI and bulk technologies. IEFF leads to accurate performance prediction across wide Vt-range.

**Session 11: Displays, Sensors, and MEMS - Imaging Technologies**
Tuesday, December 16, 9:00 a.m.
Continental Ballroom 1 – 3
Co-Chairs: Francois Roy, STMicroelectronics
Hiroaki Fujita, Eastman Kodak Company

9:00 a.m.
Introduction
9:05 a.m.
**11.1 A 36x48mm$^2$ 48M-pixel CCD Imager For Professional DSC Applications,** E.-J. Manoury, W. Klaassens, H. van Kuijk, L. Meessen, A. Kleimann, E. Bogaart, I. Peters, H. Stoldt, M. Koyuncu, J. Bosiers, DALSA Professional Imaging

A 48M-pixel, 6kx8k, 36x48mm$^2$ full-frame CCD imager was developed for professional digital SLR cameras and digital camera backs. Compared to the previous generation, the pixel size was reduced by 30% from 7.2x7.2um$^2$ to 6.0x6.0 um$^2$ to meet the demands for higher resolution. Still, by improvements in technology and design, the SNR under identical exposure conditions was increased by 30%.

9:30 a.m.
**11.2 A High-Sensitivity Broadband Image Sensor using $CuInGaSe_2$ Thin Films,** O. Matsushima, K. Miyazaki, M. Takaoka, M. Moriwake, H. Takasu, S. Ishizuka*, K. Sakurai*, A. Yamada*, S. Niki*, Rohm Corporation Limited, *National Institute of Advanced Industrial Science & Technology

We report a novel CMOS image sensor using $CuInGaSe_2$ thin films. The combination of LSI and solar cell technologies has realized a novel CMOS image sensor that outperforms conventional crystalline Si CMOS image sensors. The newly developed $CuInGaSe_2$ thin film image sensor shows considerable higher sensitivity and wider spectral range.

9:55 a.m.
**11.3 Setting up 3D Sequential Integration for Back-Illuminated CMOS Image Sensors with Highly Miniaturized Pixels with Low Temperature Fully Depleted SOI Transistors,** P. Coudrain, X. Gagnard, C. Leyris, Y. Cazaux*, B. Giffard*, P. Magnan**, P. Ancey, STMicroelectronics, *CEA LETI-MINATEC, **Institut Superiéur de l'Aéronautique et de l'Espace

We present a comprehensive study of 3D sequential technology having the capabilities to become a breakthrough in CIS miniaturization. Back-illuminated pinned photodiodes are constructed on SOI, while part of the pixel transistors is processed on a second SOI layer with $HfO_2$/TiN gates at low temperature, targeting low noise levels.

10:20 a.m.
**11.4 Advanced Image Sensor Technology For Pixel Scaling Down Toward 1.0µm (Invited),** J.C. Ahn, C.-R. Moon, B. Kim, Y. Kim, M. Lim, W. Lee, H. Park, K. Lee, K. Moon, J. Yoo, Y.J. Lee, B.J. Park, S. Jung, J. Lee, T.-H. Lee, Y.K. Lee, J. Jung, J.-H. Kim, T.-C. Kim, H. Cho, D. Lee, Y. Lee, Samsung Electronics

As pixel size of image sensors shrinks down toward 1.0um, we are reaching technical barrier to get the required YSNR10 performance. To overcome such a barrier, integration of advanced technologies such as back-side illumination, WC CFA, EDoF technologies, etc. are described and improvement for small pixel size is estimated.

10:45 a.m.
**11.5 A Wireless-Compatible Optics-Free CMOS µArray Imager,** M. Anwar, P. Matsudaira*, Whitehead Institute for Biomedical Research, *Massachusetts Institute of Technology

Optical-based bioassays are increasing important, but imagers are prohibitively expensive. We present a low-cost CMOS-based array reader that eliminates the need for optical filters and lenses, and incorporates wireless compatibility, enabling integration of the imager directly into the assay environment. We demonstrate its utility by detecting streptavidin using an array.

11:10 a.m.
**11.6 Flexible Terahertz Metamaterials: Towards a Terahertz Metamaterial Invisible Cloak,** H. Tao, N.I. Landy*, K. Fan, A.C. Strikwerda, W.J. Padilla*, R.D. Averitt, X. Zhang, Boston University, *Boston College

We have fabricated resonant terahertz metamaterials on free standing polyimide substrates with excellent mechanical flexibility and robustness. Our results provide a path forward for creating multi-layer non-planar metamaterials at terahertz frequencies, and serve as an important step forward in constructing a functional THz cloak of invisibility.

**Session 12 : Memory Technology - Resistive Memory and Magnetic Memory**
Tuesday, December 16, 9:00 a.m.
Continental Ballroom 4
Co-Chairs: Tzu-Ning Fang, Spansion Inc.
Tsugutoshi Sakamoto, NEC Corporation

9:00 a.m.
Introduction
9:05 a.m.
**12.1 Electrochemical and Thermochemical Memories (Invited),** R. Waser, RWTH University and Research Center

The review provides a survey of non-volatile, highly scalable memory devices which are based on electrochemical and thermochemical phenomena controlling the resistance of nanoscale memory cells. The classification of the memory effects, the understanding of the underlying mechanisms and a sketch of the integration efforts will be presented.

9:30 a.m.
**12.2 Highly Reliable $TaO_x$ ReRAM and Direct Evidence of Redox Reaction Mechanism,** Z. Wei, Y. Kanzawa, K. Arita, Y. Katoh, K. Kawai, S. Muraoka, S. Mitani, S. Fujii, K. Katayama, M. Iijima, T. Mikawa, T. Ninomiya, R. Miyanaga, Y. Kawashima, K. Tsuji, A. Himeno, T. Okada, R. Azuma, K.

Shimakawa, H. Sugaya, T. Takagi, R. Yasuhara*, H. Horiba*, H. Kumigashira*, M. Oshima*, Matsushita Electric Ind., Co., Ltd., *The University of Tokyo

Highly reliable $TaO_x$ ReRAM with endurance over 1E+9 cycles and retention exceeding 10 years at 85-centigrade are successfully demonstrated. $TaO_x$ exhibits stable high and low resistance states based on the redox reaction mechanism, confirmed by HX-PES directly for the first time. An 8 kbit array shows a good operating window.

9:55 a.m.
**12.3 Low Power and High Speed Bipolar Switching with A Thin Reactive Ti Buffer Layer in Robust $HfO_2$ Based RRAM,** H.Y. Lee, P.S. Chen*, T.Y. Wu**, Y.S. Chen**, C.C. Wang**, P.J. Tzeng**, C.H. Lin**, F. Chen**, C.H. Lien, M.-J. Tsai**, National Tsing Hua University, *MingShin University of Science & Technology, **Industrial Technology Research Institute

Using a thin Ti layer as the reactive buffer layer into the anodic side of memory cell, a novel $HfO_2$-based resistive memory based on 0.18μm CMOS technology is reported. Excellent and reliable memory performances are demonstrated in our memory device and promise its application in the next generation nonvolatile memory.

10:20 a.m.
**12.4 Evidence For Threshold Switching In The Set Process Of Nio-Based RRAM And Physical Modeling For Set, Reset, Retention And Disturb Prediction,** C. Cagli, D. Ielmini, F. Nardi, A.L. Lacaita, Politecnico di Milano

We provide evidence for threshold switching triggering the set transition in NiO-based RRAMs and develop a new analytical model for set. Physical set/reset models are validated by data over more than 10 decades of time, highlighting over-reset at high voltage and providing retention and disturb extrapolations for NiO-based RRAMs.

10:45 a.m.
**12.5 A Statistical Study Of Magnetic Tunnel Junction For High-Density Spin Torque Transfer-MRAM (STT-MRAM),** R. Beach, T. Min, C. Horng, Q. Chen, P. Sherman, S. Le, K. Yang, H. Yu, X. Lu, W. Kula, T. Zhong, R. Xiao, A. Zhong, G. Liu, J. Ken, J. Yuan, J. Chen, R. Tong, J. Chen, T. Torng, P. Wang, M. Chen, S. Assefa*, M. Qazi**, J. DeBrosse**, M. Gaidis*, S. Kanakasabaphathy*, Y. Lu*, J. Nowak*, E. O'Sullivan*, T. Maffitt**, J. Sun*, W.J. Gallagher*, MagIC Technologies, Inc., *IBM Research, **IBM Systems and Technology Group

For the first time, we have demonstrated a robust magnetic tunnel junction (MTJ) with a resistance-area product RA=5 $\Omega$-$\mu m^2$ that simultaneously satisfies the statistical requirements of high tunneling magnetoresistance TMR > 15 $\sigma$(Rp), write threshold spread $\sigma$ (Vw)/mean(Vw)<7.1%, breakdown-write voltage margin over 0.5V, read induced disturbance rate below 1e-9, and sufficient write endurance, and is free of unwanted write-induced magnetic reversal. The statistics suggest that a 64Mb chip at the 90-nm node is feasible.

11:10 a.m.
**12.6 Lower-Current And Fast Switching Of A Perpendicular TMR For High Speed And High Density Spin-Transfer-Torque MRAM,** T. Kishi, H. Yoda, T. Kai, T. Nagase, E. Kitagawa, M. Yoshikawa, K. Nishiyama, T. Daibou, M. Nagamine, M. Amano, S. Takahashi, M. Nakayama, N. Shimomura, H. Aikawa, S. Ikegawa, S. Yuasa*, K. Yakushiji*, H. Kubota*, A. Fukushima*, K. Oogane**, T. Miyazaki**, K. Ando*, Toshiba Corporation, *National Institute of Advanced Industrial Science and Technology, **Tohoku University

We demonstrated lower-current and fast switching of a perpendicular TMR for spin-transfer torque using a cell with 50nm diameter. An alloy with damping constant of about 0.03 was used as a free layer for the TMR cell. The switching current of 49μA and the switching speed of 4 nsec were demonstrated.

**Session 13: Emerging Technologies – Nanotechnologies for Medicine and Biology**
Tuesday, December 16, 9:00 a.m.
Continental Ballroom 5
Chair: Jesus del Alamo, Massachusetts Institute of Technology

9:00 a.m.
Introduction
9:05 a.m.
**13.1 Systems Design of a High Resolution Retinal Prosthesis (Invited),** J.D. Weiland, W. Fink, M. Humayun, W. Liu**, W. Li**, M. Sivaprakasam**, Y.-C. Tai*, M.A. Tarbell*, University of Southern California, *California Institute of Technology, **University of California Santa Cruz

9:30 a.m.
**13.2 Design and Integration in Technology for Miniature Medical Micro Systems (Invited),** C. Van Hoof, H. Neves, A.A.A Aarts, F. Iker, P. Soussan, M. Gonzales, E. Beyne, J. Vanfleteren, R.P. Puers*, P. De Moor, IMEC, * and K.U. Leuven

9:55 a.m.
**13.3 Microelectronics Meets the Brain: Towards Implantable Neural Communication Interfaces (Invited),** Y.-K. Song, D.A. Borton, S. Park, W.R. Patterson, C.W. Bull, J. Mislow, J. Simeral, J.P. Donoghue, A.V. Nurmikko, Brown University

10:20 a.m.
**13.4 Electronic Systems and New Pharmaceutical Therapies and Diagnostics (Invited),** N.M. Elman, Y. Patta, A.W. Scott, B.C. Masi, H.L.Ho Duc, G. Kim, K. Daniel, C.C. Vassiliou, M.J. Cima, Massachusetts Institute of Technology

10:45 a.m.
**13.5 Silicon Nanowires for Bioadhesive Drug Delivery (Invited),** K. Fischer, S. Tao*, H. Daniels*, E. Li**, T. Desai, University of California San Francisco, *Charles Stark Draper Laboratories, and **Nanosys

**Session 14: Characterization, Reliability, and Yield - ESD/Memory Reliability**
Tuesday, December 16, 9:00 a.m.
Continental Ballroom 6
Co-Chairs: Harald Gossner, Infineon Technologies AG
Alessandro Paccagnella, University of Padova

9:00 a.m.
Introduction
9:05 a.m.
**14.1 ESD Qualification Changes for 45nm and Beyond (Invited),** C. Duvvury, Texas Instruments Inc.

As the silicon technologies advance further into sub-50nm features sizes, the circuit demands for high-speed operation are continually making ESD into a challenging issue. This paper reviews the current perception about ESD and why there must be an immediate paradigm shift for the ESD qualification requirements.

9:30 a.m.
**14.2 Impact of Strain on ESD Robustness of FinFET Devices,** A. Griffoni, S. Thijs, C. Russ**, D. Tremouilles^, M. Scholz, D. Linten, N. Collaert, R. Rooyackers, C. Duvvury^^, H. Gossner**, G. Meneghesso*, G. Groeseneken, IMEC, *University of Padova, **Infineon Technologies AG, ^LAAS/CNRS, ^^Texas Instruments Inc.

The ESD performance of multi-gate NMOS devices is investigated in both active MOS-diode and parasitic-bipolar mode, highlighting the impact of strained SiN layers. Strain improves the ESD robustness up to 30 % in multi-fin FinFETs. A different failure mechanism is discovered in strained devices.

9:55 a.m.
**14.3 Guard Ring Interactions and their Effect on CMOS Latchup Resilience,** F. Farbiz, E. Rosenbaum, University of Illinois at Urbana-Champaign

Latchup resilience is studied by considering interactions between multiple carrier collectors and N or P-type guard rings. It is shown that P-type taps and guard rings have a deleterious effect on latchup. Physical explanations are provided based on measurements in 90 and 130nm technologies as well as extensive device simulations.

10:20 a.m.
**14.4 A Novel Method For Evaluating Electron/Hole Mismatch In Scaled Split-Gate SONOS Memories,** Y. Tsuji, M. Terai, S. Fujieda, T. Syo*, T. Saito*, K. Ando*, NEC Corporation, *NECEL Corporation

A new simple method for lateral charge profiling of split-gate SONOS memory was developed to separate trapped charge densities near and far from drain. Retention loss due to electron/hole mismatch is successfully reproduced with two hole components near and far from the drain that this method evaluates.

10:45 a.m.
**14.5 Statistical Investigation of the Floating Gate Memory Cell Leakage through High-k Interpoly Dielectrics and Its Impact on Scalability and Reliability,** B. Govoreanu, R. Degraeve, J. Van Houdt, G. Jurczak, IMEC

We investigate the floating gate cell leakage through high-k IPDs, using a statistical approach. Experimentally extracted trap distributions are used together with a newly developed Monte-Carlo leakage/retention simulator to study the impact of single- and multitrap leakage paths on scaled cells and predict the failure rate on Flash memory arrays.

11:10 a.m.
**14.6 Neutron-Induced Soft Errors In Advanced Flash Memories,** G. Cellere[1], S. Gerardin[1], M. Bagatin[1], A. Paccagnella[1], A. Visconti[2], M. Bonanomi[2], S. Beltrami[2], P. Roche[3], G. Gasiot[3], R. Harboe Sorensen[4], A. Virtanen[5], C. Frost[6], P. Fuochi[7], C. Andreani[8], G. Gorini[9], A. Pietropaolo[9], S. Platt[10], [1]Padova University, [2]Numonyx R&D, [3]STMicroelectronics, [4]ESA/ESTEC, [5]University of Jyvaskyla, [6]Rutherford Appleton Laboratory, [7]CNR-ISOF, [8]Universita di Roma Tor Vergata, [9]University di Milano, [10]University of Central Lancashire

We demonstrate Soft Errors induced by atmospheric neutrons in Flash memories and we provide an explanation linked to the physics of the neutron-matter interaction. The neutron sensitivity is expected to increase for future technologies, but the Soft Error issue is and will be within the limit of ECC capabilities.

**Session 15: Quantum, Power, and Compound Semiconductors Devices - III-V MOSFETs with High K Dielectrics**
Tuesday, December 16, 9:00 a.m.
Continental Ballroom 7 – 9
Co-Chairs: Patrick Fay, University of Notre Dame
Isik Kizilyalli, ALTA Devices

9:00 a.m.
Introduction
9:05 a.m.
**15.1 Addressing The Gate Stack Challenge For High Mobility $In_xGaAs$ Channels For NFETs,** N. Goel, D. Heh*, S. Koveshnikov, I. Ok*, S. Oktyabrsky**, V. Tokranov**, R. Kambhampati**, M.

Yakimov**, Y. Sun^, P. Pianetta^, C.K. Gaspe^^, M.B. Santos^^, J. Lee[#], P. Majhi, W. Tsai, Intel, *SEMATECH, **University at Albany-State University of New York, ^SSRL, ^^University of Oklahoma, [#]University of Texas at Austin

Through evaluation of various dielectrics, we address key gate stack issues including a) EOT scalability for high performance and electrostatic control with acceptable leakage at operating and off-state, b) understand impact of charge trapping, c) thermal stability on InGaAs, and d) impact of In% on interface on surface channel MOSFETs.

9:30 a.m.
**15.2 Scaling of $In_{0.7}Ga_{0.3}As$ Buried-Channel MOSFETs,** Y. Sun, E.W. Kiewra, J.P. de Souza, J.J. Bucchignano, K.E. Fogel, D.K. Sadana, G.G. Shahidi, IBM T.J. Watson Research Center

Sub-100-nm short-channel $In_{0.7}Ga_{0.3}As$ MOSFETs are demonstrated for both depletion- and enhancement-mode devices. High current of 960 μA/μm and record transconductance of 793 μS/μm have been achieved. Scaling behavior is investigated down to 80 nm for the first time in III-V MOSFETs. Good scaling behavior is observed for on-state current, transconductance, as well as the virtual source velocity.

9:55 a.m.
**15.3 High-Performance Surface Channel In-Rich $In_{0.75}Ga_{0.25}As$ Mosfets With ALD High-*K* As Gate Dielectric,** Y. Xuan, T. Shen, M. Xu, Y.Q. Wu, P. D. Ye, Purdue University

We demonstrated high-performance surface channel $In_{0.75}Ga_{0.25}As$ NMOSFETs using ALD $Al_2O_3$ as gate dielectric with maximum inversion current of 1.0 A/mm and electron velocity of $1.0x10^7$ cm/s at 0.75-μm gate-length. $In_{0.53}Ga_{0.47}As$, $In_{0.65}Ga_{0.35}As$ and $In_{0.75}Ga_{0.25}As$ NMOSFETs are systematically studied indicating indium-riched InGaAs could be an ideal channel material for ultimate CMOS applications.

10:20 a.m.
**15.4 Approaching Fermi Level Unpinning In Oxide-$In_{0.2}Ga_{0.8}As$,** T.H. Chiang, W.C. Lee, K.H. Shiu, D. Lin**, T.D. Lin, J. Kwo, W.E. Wang*, W. Tsai*, M. Hong, National Tsing Hua University, *Intel Corp., **Purdue University

C-V measurements under light illumination and under wide range of temperatures have been performed on UHV- deposited $Al_2O_3$(3nm)/$Ga_2O_3$ ($Gd_2O_3$)(8.5nm) on n- and p-$In_{0.2}Ga_{0.8}As$/GaAs. The results exhibit very high-quality interface and free-moving Fermi-level near the band-edges (regions close to Ec and Ev), setting a new benchmark for III-V InGaAs passivation.

10:45 a.m.
**15.5 Multi-Probe Interface Characterization of $In_{0.6}5Ga_{0.3}5As/Al_2O_3$ MOSFET,** D. Varghese, Y. Xuan, Y.Q. Wu, T. Shen, P.D. Ye, M.A. Alam, Purdue University

Using a combination of measurement techniques and simulation we show that the nature of the interface trap - and not the number alone - determines the Fermi level pinning and surface inversion. The $In_{0.65}Ga_{0.35}As$/ $Al_2O_3$ MOSFET shows strong inversion characteristics despite the relatively high interface trap densities as majority of the traps are donor-like.

11:10 a.m.
**15.6 A New Silane-Ammonia Surface Passivation Technology for Realizing Inversion-Type Surface-Channel GaAs N-MOSFET with 160 nm Gate Length and High-Quality Metal-Gate/High-k Dielectric Stack,** H.-C. Chin, M. Zhu, Z.-C. Lee, X. Liu, K.-M. Tan, H.K. Lee*, L. Shi*, L.-J. Tang**, C.-H. Tung**, L.-S. Tan, Y.-C. Yeo, National University of Singapore, *Data Storage Institute, **Institute of Microelectronics

We report a novel surface passivation technology employing a silane-ammonia gas mixture to realize very high quality high-k gate dielectric on GaAs. Interface state density $D_{it}$ of ~1x $10^{11}$ $eV^{-1}cm^{-2}$ was achieved, which is the lowest reported value for a high-k dielectric formed on GaAs by CVD, ALD, or PVD

techniques. We also realized the smallest reported (160 nm gate length) inversion-type enhancement-mode surface channel GaAs MOSFET. One of the highest peak electron mobility of ~2100 $cm^2$/V-s for surface-channel GaAs MOSFET was achieved. Extensive bias-temperature instability (BTI) characterization was performed to evaluate gate dielectric reliability.

**Session 16: Process Technology - Ge-Channel CMOS and Advanced Gate Stacks**
Tuesday, December 16, 9:00 a.m.
Imperial Ballroom
Co-Chairs: Anand Murthy, Intel
Kentaro Shibahara, Hiroshima University

9:00 a.m.
Introduction
9:05 a.m.
**16.1 Low Temperature (≤380ºC) and High Performance Ge CMOS Technology with Novel Source/Drain by Metal-Induced Dopants Activation and High-K/Metal Gate Stack for Monolithic 3D Integration,** J.-H. Park, M. Tada, D. Kuzum, P. Kapur, H.-Y. Yu, H.-.S.P. Wong, K.C. Saraswat, Stanford University

We demonstrate high performance, 3D IC compatible, Ge n and pMOSFETs with high-K/metal gate stack and novel S/D junctions by Co-induced dopant activation at below 380ºC. Very low series resistance and shallow S/D junctions are achieved. Besides, the Ge n and pMOSFETs provide an excellent $I_{on}/I_{off}$ ratio ($\sim 1.10^3$).

9:30 a.m.
**16.2 High Mobility High-k/Ge pMOSFETs with 1 nm EOT - New Concept on Interface Engineering and Interface Characterization,** R. Xie, T.H. Phung, W. He, Z. Sun, M. Yu*, Z. Cheng**, C. Zhu, National University of Singapore, *Institute of Microelectronics, **AmberWave Systems

A new concept of post-gate treatment for interface engineering is demonstrated together with $GeO_2$ surface passivation. Record high drive current and high mobility Ge-pMOSFETs with 1nm EOT have been demonstrated. Interface properties for Ge-MOSFETs have been investigated using variable rise/fall time charge-pumping method under room temperature for the first time.

9:55 a.m.
**16.3 Localized Ultra-Thin Geoi: An Innovative Approach To Germanium Channel Mosfets On Bulk Si Substrates,** E. Batail, S. Monfray, C. Tabone*, O. Kermarrec, J.F. Damlencourt*, P. Gautier*, G. Rabille*, C. Arvet, N. Loubet, Y. Campidelli, J.M. Hartmann*, A. Pouydebasque*, V. Delaye*, C. Le Royer*, G. Ghibaudo**, T. Skotnicki, S. Deleonibus*, STMicroelectronics, *CEA-LETI MINATEC, **IMEP-LAHC Minatec

We report in this paper the first demonstration of highly performant Localized GeOI transistors. We compared two integration schemes, based first on (i) the Ge-condensation process and (ii) the epitaxy of a pure ultra-thin Ge layer (capped by Si) on Si. WIth this second approach, we demonstrated for the first time functional localized GeOI pMOS transistors down to 75nm gate length, with drive current up to 600µA/µm @-1.1V.

10:20 a.m.
**16.4 Plasma PH3-Passivated High Mobility Inversion InGaAs MOSFET Fabricated with Self-Aligned Gate First Process and $HfO_2$/TaN Gate Stack,** J. Lin, S.J. Lee, H.-J. Oh, W. Yang, G.Q. Lo*, D.L. Kwong*, D.Z. Chi**, National University of Singapore, *Institute of Microelectronics, **Institute of Materials Research and Engineering

InGaAs MOS device are fabricated using TaN/High-k gate stacks. PH3-passivated MOS capacitances achieved EOT=1.7nm, $J_g$=2 X $10^{-5}$A/$cm_2$. S/D is activated by 600ºC RTA. Inversion nMOSFET with PH3-

passivation exhibits a record S.S.=96mV/dec, $\mu_{eff}$=1600cm$^2$/Vs, four-time reduction in S.S. and significant leap in drain current comparing to recent reports. Sub 100nm InGaAs MOSFET is demonstrated.

10:45 a.m.
**16.5 Fluorinated $HfO_2$ Gate Dielectrics Engineering for CMOS by Pre- and Post-CF4 Plasma Passivation,** W.-C. Wu, C.-S. Lai*, S.-C. Lee, M.-W. Ma, T.-S. Chao, J.-C. Wang*, C.-W. Hsu, P.-C. Chou*, J.-H. Chen, K.-H. Kao, W.-C. Lo, T.-Y. Lu, L.-L. Tay**, N. Rowell**, National Chiao Tung University, *Chang Gung University, **National Research Council of Canada

In this paper, we demonstrate TaN/Fluorinated $HfO_2$ CMOS devices, focusing on symmetry and asymmetry fluorine incorporation at top or bottom $HfO_2$ interfaces. 16% permittivity enhancement, 65% and 91% mobility increases for electron and hole, respectively, under high electric field was achieved. Reliability of n- and p-MOSFET was improved 3 orders and 8% for GIDL and hot carrier immunity, respectively. A physical model of shallow and deep trapping level affected by fluorine was proposed to explain the NBTI and PBTI improvements.

11:10 a.m.
**16.6 Impact of Additional Factors in Threshold Voltage Variability of Metal/High-k Gate Stacks and Its Reduction by Controlling Crystalline Structures and Grains in the Metal Gates,** K. Ohmori, T. Matsuki*, D. Ishikawa*, T. Morooka*, T. Aminaka*, Y. Sugita*, T. Chikyow**, K. Shiraishi^, Y. Nara*, K. Yamada, Waseda University, *SELETE, **National Institute for Materials Science, ^University of Tsukuba

We have clarified that in a metal/high-k gate stack, the threshold voltage variability (TVV) is attributed to crystal structures and grain sizes in the metal gate, which arises additional variability factor to the conventional random dopant fluctuation (RDF). We have successfully eliminated such additional factor by directed reduction of grain size in the metal gate. We demonstrate that a C-incorporation into TiN metal gates, which transforms the crystalline film into amorphous, is effective for reducing the TVV values in HfSiON pFET devices. We confirmed that the TVV values of C-incorporated TiN devices are determined by RDF, demonstrating that the additional TVV factor by metal gate is eliminated.

## Luncheon Session

**Tuesday, December 16, 12:20 p.m.**
**Grand Ballroom B**

*Luncheon Presentation:* *"Educating Engineers for the 21st Century"*
*James D. Plummer, Stanford University*

Undergraduate engineering education for more than 50 years has been aimed at producing graduates who are immediately productive at the companies that employ them. This objective is quite distinct from other professions like business, law and medicine, that encourage a broad liberal arts undergraduate education followed by several years of specialized graduate training. In many developed countries today, including the US, Europe and Japan, student interest in engineering is declining, in contrast to developing countries like China and India, in which student interest in engineering is exploding.

How should we educate students today for engineering careers in an increasingly global, flat world? Is packing as much detailed technical material as possible into an undergraduate major the best strategy? Or should we put more emphasis on quantitative reasoning, entrepreneurship, creativity, innovation, systems integration, working in teams and other skills that many believe are critical for success in this century? Should we rely more on graduate education for the detailed technical skills engineers need?

These questions are being debated in engineering schools today. This talk will attempt to assess these issues and draw some conclusions. The outcomes of this debate may have significant consequences for the industry-university partnership that is so important for engineering schools today.

Jim Plummer is Dean of Engineering and Professor of Electrical Engineering at Stanford University. Prior to becoming Dean, he was the chair of the EE department at Stanford. He received his BSEE degree from UCLA and MS and Ph.D. degrees in EE from Stanford.

Dr. Plummer is a member of the National Academy of Engineering, the American Academy of Arts and Sciences, and a Fellow of the IEEE. He has received a number of awards for his research including, the 1991 Solid State Science and Technology Award from the Electrochemical Society, the 2001 Semiconductor Industry Association University Research Award, the 2003 IEEE Ebers Award and the 2007 IEEE Andrew S. Grove Award. He has graduated over 80 Ph.D. students with whom he has published more than 400 journal and conference papers. These papers have won 8 conference and student best paper awards. Most of his graduated students work in the semiconductor industry. He has also received three teaching awards at Stanford. He serves on the Board of Directors of several public and start-up companies including Intel. His primary research interests are in nanoscale silicon devices.

**Awards Presentation**

*2008 IEEE Cledo Brunetti Award*
*2008 IEEE Andrew S. Grove Award*
*2008 IEEE Frederik Philips Award*
*2008 IEEE Leon K. Kirchmayer Graduate Teaching Award*

**Session 17 : Special Session - Issues at the Confluence of Technology and Design**
Tuesday, December 16, 2:15 p.m.
Grand Ballroom A
Chair: Vivek Subramanian, University of California, Berkeley

2:20 p.m.
**17.1 Technology-Circuit Collaboration for Low Power LSI (Invited),** Takayasu Sakurai, University of Tokyo

2:45 p.m.
**17.2 Design and Use of Tweakable Devices for Future Logic Implementation (Invited),** Puneet Gupta, University of California, Los Angeles

3:10 p.m.
**17.3 Taking the Next Step in Moore's Law: Designs Turn to Enable Next Technology Node (Invited),** Andrzej Strojwas, Carnegie-Mellon University and PDF Solutions

3:35 p.m.
**17.4 Advanced Simulation of Statistical Variability and Reliability in Nano CMOS Transistors (Invited),** Asen Asenov, University of Glasgow

4:00 p.m.
**17.5 Designing Robust Ultra-Low Power Circuits (Invited),** Dennis Sylvester, University of Michigan

4:25 p.m.
**17.6 Designing Temperature Sensors in Standard CMOS (Invited),** Kofi Makinwa, Technical University, Delft

4:50 p.m.
**17.7 Circuit-Driven Requirements for CMOS-Replacement Devices (Invited),** Mark Horowitz, Elad Alon*, Tsu-Jae King*, Stanford University, *University of California, Berkeley

**Session 18: Characterization, Reliability, and Yield - Strain Optimization and Performance**
Tuesday, December 16, 2:15 p.m.
Continental Ballroom 1 – 3
Co-Chairs: Ramgopal Rao, IIT Bombay
Gilles Reimbold, CEA-LETI

2:15 p.m.
Introduction
2:20 p.m.
**18.1 Strain Mapping Technique for Performance Improvement of Strained MOSFETs with Scanning Transmission Electron Microscopy,** N. Nakanishi, S. Kudo, M. Kawakami, T. Hayashi, H. Oda, T. Uchida, Y. Miyagawa, K. Asai, K. Ohnishi, N. Hattori, Y. Hirose, T. Koyama, K. Asayama, E. Murakami, Renesas Technology Corp.

A new approach of strain mapping is proposed with scanning transmission electron microscopy and applied to strained MOSFETs. This technique is extended to quantitative strain measurement with maximum spatial resolution. This technique is utilized for improving the performance and optimizing stress design for strained MOSFETs of 45 nm node and beyond.

2:45 p.m.
**18.2 More Strain and Less Stress- The Guideline for Developing High-End Strained CMOS Technologies with Acceptable Reliability (Invited),** S.S. Chung, E.R. Hsieh, D.C. Huang, C.S. Lai, C.H. Tsai, P.W. Liu, Y.H. Lin, C.T. Tsai, G.H. Ma, S.C. Chien, S.W. Sun

The design guideline with emphasis on CMOS device reliability has been addressed. Advanced 65nm CMOS devices with various strains were evaluated. For strained pMOSFETs, both uniaxial and biaxial devices have been studied. For the first time, an interface trap profiling, suitable for HC and NBTI analyses, has been developed by an improved DCIV method. Uniaxial-strained device shows better reliability. For the strained nMOSFETs, SiGe-channel device suffers from the Ge out-diffusion. SSOI exhibits good hot-carrier immunity. The SiC on S/D device is a potential candidate while its junction leakage is serious. CESL device seems to be a good and mature strain silicon technology in terms of performance, reliability, and process simplicity.

3:10 p.m.
**18.3 Trimming of IC Timing and Delay by Backside FIB Processing - Comparison of Conventional and Strained Technologies,** R. Schlangen, R. Leihkauf, T. Lundquist*, P. Egger**, C. Boit, Berlin University of Technology, *DCG Systems Inc., **Infineon Technologies AG

Rapid prototyping options provided by backside FIB preparation are expanded by trimming device delay to the desired quantity. Proper FIB treatment of 180nm CMOS is demonstrated speeding up or slowing down devices by more than 20%, which agrees well with simulations. Strained 65nm devices show an even increased effect.

3:35 p.m.
**18.4 A New Framework for Performance Prediction of Advanced MOSFETs with Plasma-Induced Recess Structure and Latent Defect Site,** K. Eriguchi, Y. Nakakubo, A. Matsuda, M. Kamei, H. Ohta, H. Nakagawa*, S. Hayashi*, S. Noda*, K. Ishikawa*, M. Yoshimaru*, K. Ono, Kyoto University, *Semiconductor Technology Academic Research Center

This paper clarifies the recess structure formation by employing a molecular dynamics simulation, and quantifies the latent defect density identified beneath the recess by using novel techniques, and the defect-depth distribution by a profile simulation. We demonstrate a framework for performance prediction by plasma parameters in MOSFETs damaged by plasma.

4:00 p.m.

**18.5 Effects Of Drain Bias On Threshold Voltage Fluctuation And Its Impact On Circuit Characteristics,** M. Miyamura, T. Nagumo*, K. Takeuchi*, K. Takeda*, M. Hane*, NEC Corporation, *NEC Elecrtronics Corporation

Enhancement mechanism of Vth fluctuation in saturation region is analyzed through addressable transistor array measurement and 3D Monte-Carlo TCAD simulation. Random dopant fluctuation in heavily doped halo devices enhances source-drain asymmetry, resulting in non-Gaussian distribution of DIBL and saturation Vth. Its impact on SRAM stability is also evaluated.

**Session 19: Quantum, Power, and Compound Semiconductors Devices - RF Power and Optoelectronic Devices**
Tuesday, December 16, 2:15 p.m.
Continental Ballroom 4
Co-Chairs: Enrico Zanoni, Università di Padova
Vishnu Khemka, Freescale Semiconductor Inc.

2:15 p.m.
Introduction
2:20 p.m.
**19.1 High RF Power Transistor With Laterally Modulation-Doped Channel And Self-Aligned Silicide In 45nm Node CMOS Technology,** M. Shima, T. Suzuki, Y. Kawano, K. Okabe*, S. Yamaura, K, Joshin, T. Futatsugi, Fujitsu Laboratories Ltd., *Fujitsu Microelectronics Limited

A novel low on-resistance and high RF power transistor was developed to integrate high RF power amplifier. A self-aligned silicide and laterally modulation-doped channel attained the lowest on-resistance of 1.7 Ω—-mm with high breakdown voltage of more than 10 V and successfully achieved the highest output power density of 0.6 W/mm.

2:45 p.m.
**19.2 A CMOS-Compatible, High RF Power, Asymmetric-LDD MOSFET with Excellent Linearity,** T. Chang, H.L. Kao*, Y.J. Chen, S.L. Liu, S.P. McAlister**, A. Chin, National Chiao-Tung University, *Chang Gung University, **National Research Council of Canada

Using novel Asymmetric-LDD design, the 0.18 um RF power MOSFET shows twice DC breakdown voltage of 6.9 V, much better 0.54 W/mm power density, higher 115 GHz $f_{max}$, improved ACPR linearity as much as 8 dB and high 52% drain efficiency at 2.4 GHz than conventional MOSFET.

3:10 p.m.
**19.3 Impact Of Electrical Degradation On Trapping Characteristics Of Gan High Electron Mobility Transistors,** J. Joh, J. del Alamo, Massachusetts Institute of Technology

One of the most deleterious effects of electrical degradation of GaN HEMTs is an increase in carrier trapping and subsequent current collapse. In this work, we have investigated the trapping and detrapping characteristics of GaN HEMTs before and after device degradation through a new current transient analysis methodology.

3:35 p.m.
**19.4 Silicon Photonic Modulator and Integration for High-speed Applications (Invited),** L. Liao, A. Liu, J. Basak, H. Nguyen, M. Paniccia, Y. Chetrit*, D. Rubin*, Intel Corporation, *Numonyx Israel Ltd.

As microprocessor technology advancements continuously drive the need for high-bandwidth I/O, optical interconnect has become a subject of increasing interest. We present recent results of a silicon photonic integrated chip that contains an array of silicon optical modulators in a wavelength division multiplexing design. Using a single multi-wavelength laser source, we demonstrate aggregate data transmission of 200 Gbps.

4:00 p.m.
**19.5 Observation of Optical Gain in Ultra-Thin Silicon Resonant Cavity Light-Emitting Diode,** S. Saito, N. Sakuma, Y. Suwa, H. Arimoto, D. Hisamoto, H. Uchiyama, J. Yamamoto, T. Sakamizu, T. Mine, S. Kimura, T. Sugawara, M. Aoki, T. Onai, Hitachi Ltd.

We have fabricated an ultra-thin Si resonant cavity light-emitting diode by CMOS and MEMS process. The photoluminescence spectra show narrow resonances, and the electroluminescence intensity increases nonlinearly with currents. The optical gain is considered to be originated from intrinsic material properties of ultra-thin Si due to quantum confinements.

4:25 p.m.
**19.6 Role Of Non-Radiative Recombination In The Degradation Of Ingan-Based Laser Diodes,** M. Meneghini, N. Trivellin, L. Trevisanello, G. Meneghesso, E. Zanoni, K. Orita*, M. Yuri*, D. Ueda*, University of Padova, Matsushita Electric Ind. Ltd.

This paper presents an analysis of the degradation of InGaN-based laser diodes, carried out by means of combined electro-optical techniques. For the first time, we demonstrate that the increase of the threshold current is strongly correlated to the decrease of the non-radiative recombination lifetime in the active region.

4:50 p.m.
**19.7 Single-Crystal Thin-Film Bonding on Diamond-Like Carbon Film by Intermolecular Force for Super High-Density Integration of High-Power LEDs,** M. Ogihara, T. Sagimori, M. Mutoh, T. Suzuki, H. Fujiwara, M. Sakuta, Oki Digital Imaging Corporation

Bonding of single-crystal thin-film (epifilm) for LEDs on diamond-like carbon (DLC) film on the Si substrate (DLC/Si) by intermolecular-force at room temperature has been achieved for the fist time. We found that the epifilm-LED was well bonded on DLC/Si and the novel epifilm-LED/DLC/Si achieved good heat-dissipation providing very high emitted-light-powers.

**Session 20: Displays, Sensors, and MEMS - Biosensors and 3D Hetero Integration**
Tuesday, December 16, 2:15 p.m.
Continental Ballroom 5
Co-Chairs: Werner Weber, Infineon Technologies AG
Karlheinz Bock, University of Berlin

2:15 p.m.
Introduction
2:20 p.m.
**20.1 Precise Detection Of Single Mismatched DNA With Functionalized Diamond Electrolyte Solution Gate FET,** S. Kuga, S. Tajima, J.-H. Yang, K. Hirama, H. Kawarada, Waseda University

We demonstrated the DC operation of diamond SGFET and discrimination of Comp and 1MM DNA in solution. Transconductance (sensitivity) of SGFET was increased by miniaturization of FET. The ratio of change in gate potential by hybridization of Comp. and 1MM DNA was 3:1 on functionalized diamond SGFET.

2:45 p.m.
**20.2 Development Of Wafer Scale Plasmonics-Active SERS Substrates on a Wafer Scale For Chemical And Biological Sensing Applications,** A. Dhawan,Y. Du*, H. Wang, D. Leonard**, V. Misra*, M. Ozturk*, M. Gerhold^, V.-D. Tuan, Duke University, *North Carolina State University, **Appalachian State University, ^US Army Research Office

In this work we demonstrated reproducible fabrication of highly efficient plasmonics-active SERS substrates - having metallic nanowire structures with pointed geometries and sub-5 nm gap between the metallic nanowires enabling concentration of high EM fields in these regions - on a wafer-scale by a

process that is compatible with large-scale development of these substrates. These substrates were applied for detection of chemical and biological molecules.

3:10 p.m.
**20.3 Overcoming The Screening-Induced Performance Limits Of Nanowire Biosensors: A Simulation Study On The Effect Of Electro-Diffusion Flow,** Y. Liu, K. Lilja*, R.W. Dutton, Stanford University, *Robust Chip Inc.

We develop device-level simulation capabilities to self-consistently model the Si-nanowire biosensor systems. Based on our simulation study, we demonstrate that by introducing electro-diffusion current flow in the electrolyte solutions, the electrostatic screening of the biological charge by the electrolytes can be significantly suppressed. Therefore, the screening-induced performance limits of Si-nanowire biosensors can be overcome; an improvement of sensitivity by >~10X is indicated based on the proposed operation principle.

3:35 p.m.
**20.4 Through-Silicon Via and Die Stacking Technologies for Microsystems-Integration (Invited),** E. Beyne, P. De Moor, W. Ruythooren, R. Labie, A. Jourdain, H. Tilmans, D. Sabuncuoglu Tezcan, P. Soussan, B. Swinnen, R. Cartuyvels, IMEC

The highest integration density of microsystems can be obtained using a 3D-stacking approach, where each layer of the stack is realized using a different technology, which may include sensors, imagers, rf and MEMS technologies. A key challenge is however to perform such stacking in a cost-effective manner. In this paper, a novel 3D TSV and 3D stacking technologies will be presented. Application examples are MEMS packaging and heterogeneous integration of imaging devices.

4:00 p.m.
**20.5 New Heterogeneous Multi-Chip Module Integration Technology Using Self-Assembly Method,** T. Fukushima, T. Konno, K. Kiyoyama, M. Murugesan, K. Sato, W.-C. Jeong, Y. Ohara, A. Noriki, S. Kanno, Y. Kaiho, H. Kino, K. Mikito, R. Kobayashi, C.-K. Yin, K. Inamura, J.-C. Be, T. Tanaka, M. Koyanagi, Tohoku University

We have proposed heterogeneous integration technology using lateral interconnections climbing over 100-um-thick MEMS and LSI chips. By using surface tension of aqueous liquid, a large number of chips were simultaneously and precisely self-assembled onto substrates with a high alignment accuracy of approximately 400 nm on average. The lateral interconnections were three-dimensionally formed from contact pads on chip upside to electrodes on the substrates along chip sidewall. We obtained excellent electrical characteristics of the lateral interconnections and we successfully confirmed the basic operation of ASK modulater LSI chip.

4:25 p.m.
**20.6 MEMS Vertical Probe Cards with Both Line-arrayed and Area-arrayed Ultra-dense Metal Tips for Wafer-level IC Testing,** F. Wang, R. Cheng, X. Li, Chinese Academy of Science

A novel MEMS technique is developed for probe-cards with ultra-dense vertical tips for wafer-level testing advanced ICs with various types of dense pad layout. The minimum tip pitch of 90µm x 196 µm and 50 µm for testing area-arrayed and line-arrayed pads are achieved. Satisfactory mechanical and electric performances are tested that show promise of the probe-cards for testing next generation ICs.

**Session 21: Solid State and Nanoelectronic Devices - Carbon-Based Devices**
Tuesday, December 16, 2:15 p.m.
Continental Ballroom 6
Co-Chairs: Jing Kong, Massachusetts Institute of Technology
Tsu-Jae King Liu, University of California, Berkeley

2:15 p.m.

Introduction

2:20 p.m.

**21.1 Mobility Extraction And Quantum Capacitance Impact In High Performance Graphene Field-Effect Transistor Devices,** Z. Chen, J. Appenzeller*, IBM T.J. Watson Research Center, *Purdue University

We present for the first time a room temperature direct measurement of the ballistic mean free path in graphene at carrier concentrations of above 1012cm$^{-2}$. Furthermore, we demonstrate first quantum capacitance measurements on single-layer graphene devices and elucidate on their relevance for the extraction of mobility for scaled graphene FETs.

2:45 p.m.

**21.2 RF Performance Of Top-Gated, Zero-Bandgap Graphene Field-Effect Transistors,** I. Meric, N. Baklitskaya, P. Kim, K.L. Shepard, Columbia University

We present the first experimental high-frequency measurements of graphene field-effect transistors (GFETs), demonstrating an ft of 6.4GHz for a 0.5µm-length device. We also present detailed measurement and analysis of velocity saturation in GFETs, demonstrating the potential for velocities approaching 108 cm/sec, and the effects of an ambipolar channel on current-voltage characteristics.

3:10 p.m.

**21.3 Edge Chemistry Engineering of Graphene Nanoribbon Transistors: A Computational Study,** Y. Ouyang, Y. Yoon, J. Guo, University of Florida

We present a simulation framework for assessing the performance limits of graphene nanoribbon (GNR) FETs with edges terminated by different chemical species. We find a significant effect of edge chemistry on the quantum capacitance, carrier injection velocity, channel conductance and balance between the nFET and the pFET of GNRFETs.

3:35 p.m.

**21.4 Carbon-Based Resistive Memory,** F. Kreupl, R. Bruchhaus*, P. Majewski , J.B. Philipp, R. Symanczyk, T. Happ**, C. Arndt**, M. Vogt**, R. Zimmermann**, A. Buerke**, A.P. Graham**, M. Kund, Qimonda AG, *Qimonda North America, **Qimonda Dresden GmbH & Co.

We propose carbon as new resistive memory material for non-volatile memories and compare three allotropes of carbon, namely carbon nanotubes, conductive carbon and insulating carbon for their possible application as resistance-change material in high density non-volatile memories. Repetitive high-speed switching and the potential for multi-level programming have been successfully demonstrated.

4:00 p.m.

**21.5 High-Frequency Effects in Carbon Nanotube Interconnects and Implications for On-Chip Inductor Design,** H. Li, K. Banerjee, University of California Santa Barbara

This paper presents a rigorous investigation of high-frequency effects in carbon nanotube interconnects. Our analysis reveals for the first time that skin effect in CNT bundles is negligible compared to conventional metals. It is subsequently shown that CNT based inductors can achieve nearly 4X higher Q-factor than Cu based inductors.

4:25 p.m.

**21.6 Scaling and Variability Analysis of CNT-Based NEMS Devices and Circuits with Implications for Process Design,** H. Dadgour, A.M. Cassell*, K. Banerjee, University of California Santa Barbara, *NASA Ames Research Center

This work presents an extensive simulation-based scaling analysis of carbon nanotube (CNT) based Nano-Electro Mechanical Switches (NEMS) considering the effect of process variations as well as circuit level requirements for high-performance digital ICs. It is shown that CNT-NEMS structures become

increasingly vulnerable to different failure mechanisms as feature sizes scale down, thereby highlighting the need for advanced nanofabrication techniques if NEMS structures are to be used in practical digital ICs.

**Session 22: Modeling and Simulation - Atomistic Process Simulation and Memory Modeling**
Tuesday, December 16, 2:15 p.m.
Continental Ballroom 7 – 9
Co-Chairs: Ken'ichiro Sonoda, Renesas Technology Corp.
Peter Pichler, Fraunhofer IISB

2:15 p.m.
Introduction
2:20 p.m.
**22.1 Atomistic Modeling of Impurity Ion Implantation in Ultra-Thin-Body Si Devices,** L. Pelaz, R. Duffy*, M. Aboy, L. Marques, P. Lopez, I. Santos, B.J. Pawlak*, M.J.H. van Dal*, B. Duriez*, T. Merelle*, G. Doornbos*, N. Collaert**, L. Witters**, R. Rooyackers**, W. Vandervorst**, M. Jurczak**, M. Kaiser^, R.G.R. Weemaes^, J.G.M. van Berkum^, P. Breimer^, R.J.P. Lander*, University of Valladolid, *NXP-TSMC Research Center, **IMEC, ^Philips Research Laboratories Eindhoven

Source/drain formation in ultra-thin body devices by conventional ion implantation is analyzed by atomistic simulation. Dopant retention is dramatically reduced for low-energy and low-tilt angles. For the first time, Molecular Dynamics and Kinetic Monte Carlo simulations, encompassing the entire Si body, are applied to predict damage generation and recovery. These show that amorphization should be avoided as recrystallization in ultra-thin-body Si leads to twin boundary defects and poly-crystalline Si formation. Rapid dissolution of end-of range defects in thin-body Si does not significantly reduce diffusion lengths. The conclusions of the atomistic modeling are verified by a novel characterization methodology and electrical analysis.

2:45 p.m.
**22.2 Advanced 2D/3D Simulations for Laser Annealed Device using an Atomistic Kinetic Monte Carlo Approach and Scanning Spreading Resistance Microscopy (SSRM),** T. Noda, P. Eyben*, W. Vandervorst*, C. Vrancken*, E. Rosseel*, C. Ortolland*, T. Clarysse*, J. Goossens*, A. De Keersgieter*, S. Felch**, R. Schreutelkamp**, P.P. Absil*, M. Jurczak*, K. De Meyer*, S. Biesemans*, T.Y. Hoffmann*, Matsushita Electric Industrial Co. Ltd., *IMEC, **Applied Materials

Atomistic simulations and optimized TCAD strategy for Laser-only annealing device are shown. Multiple laser annealing scans are modeled by using atomistic KMC. KMC clarified that dopant diffusion is changed as a function of laser scan number. SSRM with 1 nm special resolution is used for the 2-dimensional carrier distribution measurement and active level determination.

3:10 p.m.
**22.3 Atomistic Modeling of Fluorine Implantation and Diffusion in III-Nitride Semiconductors,** L. Yuan, M. Wang, K.J. Chen, Hong Kong University of Science and Technology

A hybrid molecular dynamics/kinetic Monte Carlo model is developed for the fluorine ion implantation and diffusion in AlGaN/GaN heterostructures. The dominant F diffusion mechanism is found to be group-III substitutional to interstitial. The surface effect on the fluorine's stability and its improvement by passivation are also successfully modeled.

3:35 p.m.
**22.4 Impact Of Platinum Incorporation On Thermal Stability and Interface Resistance In NiSi/Si Junctions Based On First-Principles Calculation,** T. Marukame, T. Yamauchi, Y. Nishi, T. Sasaki*, A. Kinoshita, J. Koga, K. Kato, Toshiba Corp., *Toshiba Nanoanalysis Corporation

We studied thermal stability and reduction of interfacial resistance at Ni(Pt)Si/Si junctions based on first-principles calculations. Our calculations successfully clarified physical origin of the thermal stability of

Ni(Pt)Si. We propose the SBH modulation techniques (dipole comforting Schottky: DCS) for Ni(Pt)Si/Si junctions, being realized through implantation after silicidation processes.

4:00 p.m.
**22.5 Analytical Model for RESET Operation of Phase Change Memory,** B. Rajendran, J. Karidis, M.-H. Lee*, M. Breitwisch, G.W. Burr**, Y.-H. Shih*, R. Cheek, A. Schrott, H.-L. Lung*, C. Lam, IBM T.J. Watson Research Center, *Macronix International Co. Ltd., **IBM Almaden Research Center

We present an analytical model for RESET operation of Phase Change Memory describing the dependency of programming current on cell parameters. In addition to explaining the fundamental physics behind the inverse dependency of PCM dynamic resistance on programming current, the model shows excellent agreement with FEM simulations and experimental data.

4:25 p.m.
**22.6 A New Physics-Based Model For TANOS Memories Program/Erase,** A. Mauri, C. Monzio Compagnoni*, S. Amoroso*, A. Maconi*, F. Cattaneo, A. Benvenuti, A.S. Spinelli*, A.L. Lacaita*, Numonyx R&D, *Politecnico di Milano

In this work we present a new physics-based model able to describe the P/E transients in TANOS memories. The model is extensively validated against a large number of experimental P/E transient data taken on samples with different gate stack compositions, also as a function of temperature, and represents a useful tool for the assessment of the performance of this technology.

4:50 p.m.
**22.7 New Physical Model for Ultra-scaled 3D Nitride-Trapping Non-Volatile Memories,** E. Nowak, M. Bocquet, L. Perniola, G. Ghibaudo, G. Molas, C. Jahan, R. Kies, G. Reimbold, B. De Salvo, F. Boulanger, CEA-LETI MINATEC

A semi-analytical model tailored for nitride Charge-Trap TriGate non-volatile memories under uniform stress operation is presented. Innovations in the tunnelling current calculation at corners through the Hankel function formalism are presented. The model is validated through comparison with experimental data. Scaling opportunities of such 3D devices are deeply discussed.

5:15 p.m.
**22.8 Oxide-Based RRAM Switching Mechanism: A New Ion-Transport-Recombination Model,** B. Gao, S. Yu, N. Xu, L.F. Liu, B. Sun, X.Y. Liu, R.Q. Han, J.F. Kang, B. Yu*, Y.Y. Wang, Peking University, *NASA Ames Research Center

A new ion-transport-recombination model is proposed to quantify the switching behaviors of RRAM. The reset characteristics, such as switching speed, current, uniformity/stability of HRS and LRS, endurance, and scalability were evaluated. The proposed model provides a design guide for optimizing device structure, materials, and process of RRAM.

**Session 23: CMOS Devices and Technology - Characteristics of Mobility and Threshold Voltage in Advanced Devices**

Tuesday, December 16, 2:15 p.m.
Imperial Ballroom
Co-Chairs: Chih-Sheng Chang, TSMC
Hyungcheol Shin, Seoul National University

2:15 p.m.
Introduction
2:20 p.m.
**23.1 Carrier Transport and Stress Engineering in Advanced Nanoscale Transistors From (100) and (110) Transistors to Carbon Nanotube FETs and Beyond (Invited),** K. Uchida, M. Saitoh*, S. Kobayashi*, Tokyo Institute of Technology, *Toshiba Corporation

This paper reviews the carrier transport mechanisms and stress engineering in advanced nanoscale MOSFETs. First, carrier transport in bulk (100) and (110) MOSFETs is reviewed. We then discuss mobility in three-dimensional MOSFETs. Subband structure engineering to enhance mobility as well as ballistic current is also examined. Furthermore, future possible directions for new channel materials are addressed.

2:45 p.m.
**23.2 Comprehensive Performance Assessment of Scaled (110) CMOSFETs Based on Understanding of STI Stress Effects and Velocity Saturation,** M.Saitoh, N. Yasutake, Y. Nakabayashi, T. Numata, K. Uchida*, Toshiba Corporation, *Tokyo Institute of Technology

Origins of performance in scaled (short and narrow) (110) FETs are investigated. Idsat of scaled (110) nFETs approaches (100) nFETs due to compressive stress from STI and strong velocity saturation, while scaled (110) pFETs are superior to (100) pFETs. By suppressing Rsd, (110) CMOS shows excellent performance even without stressors.

3:10 p.m.
**23.3 Comprehensive Understanding of Surface Roughness And Coulomb Scattering Mobility in Biaxially-Strained Si MOSFETs,** Y. Zhao, M. Takenaka, S. Takagi, The University of Tokyo

We found tensile biaxial strain enhances the surface roughness scattering limited mobility of electron and degrades that of hole slightly, for the first time. It is also found that tensile biaxial strain enhances the Coulomb scattering mobility of hole induced by interface state, while degrades that induced by substrate impurity.

3:35 p.m.
**23.4 Experimental And Theoretical Analysis Of Factors Causing Asymmetrical Temperature Dependence of $V_t$ in a High-K Metal Gate CMOS With Capped High-K Techniques,** R. Iijima, M. Takayanagi*, Toshiba America Electronic Components Inc., *IBM T.J. Watson Research Center

Temperature dependence of Vt for High-k Metal CMOS is investigated thoroughly for a better understanding and prediction of Vt under real operating condition for planar FETs and FinFETs in 22nm generation and beyond.

4:00 p.m.
**23.5 On The Difference of Temperature Dependence of Metal Gate and Poly Gate SOI MOSFET Threshold Voltages,** S.-J. Han, X. Wang, P. Chang, D. Guo, M.-H. Na, K. Rim, IBM

We describe the physical origins of a higher Vt temperature sensitivity in high-k/metal gate compared to poly-Si/SiON. Distinction in temperature driven gate Fermi level shifts and poly depletion effects contribute to this difference. The impact of the floating body effect on temperature behaviors in HKMG and poly-Si/SiON SOI are described.

**Session 24 – 2008 IEDM Special Evening Session**
Tuesday, December 16, 8:00 p.m.
Continental Ballroom 1 - 4
*Session Chair:* *Roland Thewes, Qimonda*
*Highlights of ISSCC 2008*

In this Special Evening Session four outstanding papers published at the 2008 International Solid-State Circuit Conference (ISSCC) are presented to the IEDM audience. All papers are focused on the idea that circuit-technology interaction plays an important role for numerous applications, and that related circuit designs gain benefit from thorough technology understanding and vice versa.

In the first paper by Fatih Hamzaoglu et al. from Intel, OR, utilizing a 45nm high-k metal-gate CMOS technology, special emphasis is put on design-based solutions to deal with stability and leakage issues of a 153Mb SRAM with 0.346μm$^2$ cell area. Careful body biasing and implementation of sleep transistor techniques enable achievement of these goals. Whereas the first paper focuses on mainstream logic applications, the second paper by Joachim Burghartz et al. from IMS CHIPS, Stuttgart, Germany, discusses CMOS imager chips for in-vivo biomedical purposes. A sub-retinal CMOS imager implant is shown to restore vision of patients suffering from retinitis pigmentosa. Additionally, an endoscopy camera chip using an amorphous α-Si layer above standard CMOS is demonstrated. The last two papers highlight novel approaches for non-volatile memories. Ki-Tae Park et al. from Samsung, Korea, describe a multi-level 4Gb NAND Flash device in 45nm technology. High area efficiency is achieved by using two stacked Si layers providing 2Gb each. Architecture and operation issues are discussed with respect to cell properties in this 3D arrangement. The last paper by Ferdinando Bedeschi et al. from Numonyx, Italy / CA, considers a phase-change memory approach combining the properties of non-volatility and fast read and write access. A 256Mb multi-level test-chip is presented based on a 90nm microtrench technology and using $Ge_2Sb_2Te_5$ as the phase-change material.

8:00 – 8:05 p.m.
Introduction

8:05 – 8:30 p.m.
**A 153Mb-SRAM Design with Dynamic Stability Enhancement and Leakage Reduction in 45nm High-k Metal-Gate CMOS Technology,** Fatih Hamzaoglu, Kevin Zhang, Yih Wang, Hong Jo Ahn, Uddalak Bhattacharya, Zhanping Chen, Yong-Gee Ng, Andrei Pavlov, Ken Smits, Mark Bohr, Intel

8:30 – 8:55 p.m.
**CMOS Imager Technologies for Biomedical Applications,** Joachim N. Burghartz, Thorsten Engelhardt, Heinz-Gerd Graf, Christine Harendt, Harald Richter, Cor Scherjon, Karsten Warkentin, IMS CHIPS

8:55 – 9:20 p.m.
**A 45nm 4Gb 3-Dimensional Double-Stacked Multi-Level NAND Flash Memory with Shared Bitline Structure,** Ki-Tae Park, Doogon Kim, Soonwook Hwang, Myounggon Kang, Hoosung Cho, Youngwook Jeong, Yong-Il Seo, Jaehoon Jang, Han-Soo Kim, Soon-Moon Jung, Yeong-Taek Lee, Changhyun Kim, and Won-Seong Lee, Samsung

9:20 – 9:45 p.m.
**A Multi-Level-Cell Bipolar-Selected Phase-Change Memory,** Ferdinando Bedeschi, Rich Fackenthal, Claudio Resta, Enzo Michele Donze, Meenatchi Jagasivamani, Egidio Buda, Fabio Pellizzer, David Chow, Alessandro Cabrini*, Giacomo Matteo Angelo Calvi*, Roberto Faravelli*, Andrea Fantini*, Guido Torelli*, Duane Mills, Roberto Gastaldi, Giulio Casagrande, Numony, *University of Pavia

**Session 25 - 2008 IEDM Evening Panel Discussion**
Tuesday, December 16, 8:00 p.m.
Continental Ballroom 6 - 9
"The Future of Fabs"

The history of semiconductor fabs has seen exponential growth in size, volume and cost. From chemistry lab to ultra-clean, large wafer automated handling systems, the productivity increase has contributed to the sustained cost reduction as guided by Moore's law. If history were to repeat, 450mm wafer sizes would soon be here, single wafer processing would be the only tool option, and the productivity of just a few of such gigafabs would be enough to supply the smallest geometries. What factors would control this transition? Will non-optical litho be an essential element of this? What will happen to the 300mm fabs? Perhaps the change to atomic layer control dictates different processing priorities, perhaps wafers are not the only or ultimate substrate for all applications? Will the less scalable technologies like analog, or

MEMS, or (bio)medical demand a higher fraction of worldwide capacity growth? These and other questions will be discussed by a distinguished panel of fab experts from Samsung, TSMC, Toshiba, Micron, ASML, Micron, TI and Applied Materials.

Moderator: Hans Stork, CTO Silicon Systems Group, Applied Materials

**Session 26: Process Technology - Interconnect and 3D-IC Technologies**
Wednesday, December 17, 9:00 a.m.
Continental Ballroom 6 - 9
Co-Chairs: Toshiaki Hasegawa, Sony Corporation
Paul Kohl, Georgia Institute of Technology

9:00 a.m.
Introduction
9:05 a.m.
**26.1 Enabling Technologies For 3D Integration : From Packaging Miniaturization To Advanced Stacked ICs (Invited),** N. Sillon, A. Astier, H. Boutry, L. Di Cioccio, D. Henry, P. Leduc, CEA-Leti Minatec

This paper will present an overview of current 3D technologies development at CEA/LETI, and their link with applications where 3D is required. Focus will be done on the last results obtained on the key-process for 3D integration: TSV, wafer bonding, thinning & interconnects. Some electrical results obtained on different applications will be showed.

9:30 a.m.
**26.2 A 300-mm Wafer-Level Three-Dimensional Integration Scheme Using Tungsten Through-Silicon Via and Hybrid Cu-Adhesive Bonding,** F. Liu, R.R. Yu, A.M. Young, J.P. Doyle, X. Wang*, L. Shi, K.-N. Chen, X. Li*, D.A. Dipaola*, D. Brown*, C.T. Ryan*, J.A. Hagan*, K.H. Wong*, M. Lu, X. Gu, N.R. Klymko*, E.D. Perfecto*, A.G. Merryman*, K.A. Kelly*, S. Purushothaman, S.J. Koester, R. Wisnieff, W. Haensch, IBM T.J. Watson Research Center, *IBM SRDC

A 300-mm wafer-level three-dimensional integration process using tungsten through-silicon-via (TSV) and hybrid Cu/adhesive wafer bonding is demonstrated. The electrical and physical properties of the TSV and bonded interconnect are presented and show RLC values that satisfy both the power delivery and high-speed signaling requirements for high-performance 3D systems.

9:55 a.m.
**26.3 3D Stacked IC Demonstration Using a Trough Silicon Via First Approach,** J. Van Olmen , A. Mercha, G. Katti*, C. Huyghebaert, J. Van Aelst, E. Seppala, Z. Chao, S. Armini, J. Vaes, R. Teixeira Cotrin, M. Van Cauwenberghe, P. Verdonck, K. Verhemeldonck, A. Jourdain, W. Ruythooren, M. de Potter de ten Broeck, A. Opdebeeck, T. Chiarella, B. Parvais, I. Debusschere, T.Y. Hoffmann, W. Dehaene*, M. Stucchi, M. Rakowski, P. Soussan, R. Cartuyvels, E. Beyne, S. Biesemans, B. Swinnen, IMEC, *KU Leuven

We report for the first time the demonstration of 3D integrated circuits obtained by die-to-die stacking using Cu Through Silicon Vias. Functionality of various ring oscillator topologies that include inverters distributed over both top and bottom dies connected through TSVs demonstrates excellent chip integrity after TSV and 3D stacking process.

10:20 a.m.
**26.4 High Electromigration-Resistant Copper/Carbon Nanotube Composite for Interconnect Application,** Y. Chai, P.C.H. Chan, Hong Kong University of Science and Technology

We demonstrated a novel material - Cu/CNT composite, to improve the electromigration lifetime of vias and lines. Our results showed that the EM lifetime of the Cu/CNT composite is more than 5X larger than the copper with a small increase in the resistivity.

10:45 a.m.
**26.5 RF Performance Boosting for 40nm-node CMOS Device by Low-k/Cu Dual Damascene Contact,** J. Kawahara, K. Hijioka, I. Kume, H. Nagase, A. Tanabe, M. Ueki, H. Yamamoto, F. Ito, N. Inoue, M. Tagami, N. Furutake, T. Onodera, S. Saito, T. Takeuchi, T. Fukai, M. Asada, K. Arita, K. Motoyama, A. Nakajima, E. Nakazawa, R. Kitao, K. Fujii, M. Sekine, M. Ikeda, Y. Hayashi, NEC Electronics Corporation

The RF performance in 40 nm-node MOSFET devices was enhanced by the low-k/Cu DD contact. The Cu-DD structure drastically reduced the contact resistance and parasitic capacitance, boosting the $f_T$ and $f_{max}$ by 8.0 % and 10.5 % referred to the conventional $SiO_2$/W-plug contacts, respectively. The low-k/Cu DD contact is essential for the scaled-down CMOS device for RF/ubiquitous applications.

11:10 a.m.
**26.6 Comprehensive Study of 32 nm Node Ultralow-k/Cu ($k_{eff}$=2.6) Dual Damascene Integration Featuring Short TAT Silylated Porous Silica (k=2.1),** N. Oda, S. Chikaki, T. Kubota, S. Nakao, K. Tomioka, E. Soda, N. Nakamura, J. Nogawa*, Y. Kawashima*, R. Hayashi*, S. Saito, Semiconductor Leading Edge Technologies, *NEC Electronics Corporation

A comprehensive study of Ultralow-k/Cu integration featuring short TAT silylated scalable porous silica (Po-SiO, k=2.1) with high porosity (50%) is presented. Applying this improved Po-SiO, 140 nm pitch dual damascene structure is successfully achieved. The wiring capacitance showed 10 % reduction compared with the porous SiOC (ULK, k=2.65). Sufficient interconnect reliability and packaging characteristics for circuit-under-pad structure are also obtained. The predicted circuit-performance for 32 nm node is 8 % higher than that using ULK.

11:35 a.m.
**26.7 High Performance Cu Interconnects with Damage-less Full Molecular-Pore-Stack (MPS) SiOCH for 32nm-node LSIs and Beyond,** M. Ueki, M. Tagami, F. Ito, T. Onodera, I. Kume, N. Furutake, H. Yamamoto, J. Kawahara, N. Inoue, K. Hijioka, T. Takeuchi, S. Saito, N. Okada, Y. Hayashi, NEC Electronics Corporation

Damage-less full molecular-pore-stack SiOCH (MPS) / Cu interconnect is developed to reduce effective k-value. MPS with high endurance against plasma processes is introduced into both via and trench dielectrics without hard mask (HM). Low friction slurry and the chemical control of MPS surface by He-plasma treatment suppress defect generation during direct CMP of MPS surface. The full-MPS interconnect with low-k (k=3.1) cap demonstrates 10% lower inter-line capacitance and 34% lower inter-layer capacitance than the full-SiOCH (k=3.0) interconnect with SiCN-cap (k=4.9). The effective k-value $k_{eff}$ reduces to 2.67 for the damage-less full MPS structure which is applicable to 32nm LSIs and beyond.

**Session 27: CMOS Devices and Technology - Advanced CMOS Logic and SoC Platforms**
Wednesday, December 17, 9:00 a.m.
Grand Ballroom B
Co-Chairs: Seok-Hee Lee, Intel Corporation
Emmanuel Josse, STMicroelectronics

9:00 a.m.
Introduction
9:05 a.m.
**27.1 22 nm Technology Compatible Fully Functional 0.1 µm2 6T-SRAM Cell,** B. S. Haran , A. Kumar^, L. Adam, J. Chang^, V. Basker, S. Kanakasabapathy, D. Horak, S. Fan, J. Chen, J. Faltermeier, S. Seo, M. Burkhardt, S. Burns, S. Halle, S. Holmes, R. Johnson, E. McLellan, T. M. Levin, Y. Zhu, J. Kuss, A. Ebert, J. Cummings, D. Canaperi, S. Paparao, J. Arnold, T. Sparks**, C. S. Koay, T. Kanarsky, S.

Schmitz, K. Petrillo, R. H. Kim*, J. Demarest, L. Edge, H. Jagannathan, M. Smalley, N. Berliner, K. Cheng, D. LaTulipe, C. Koburger, M. Raymond*, M. Colburn, T. Spooner, V. Paruchuri, W. Haensch^, D. McHerron, B. Doris, IBM Research at Albany Nanotech, *Advanced Micro Devices, **Freescale Semiconductor, ^IBM T.J. Watson Research Center

We demonstrate 22 nm node technology compatible, fully functional 0.1 $\mu m^2$ 6T-SRAM cell using high-NA immersion lithography and state-of-the-art 300 mm tooling. This is the world's smallest 6T-SRAM cell. The cell exhibits a static noise margin (SNM) of 220 mV at VDD=0.9 V. Key enablers include band edge high-k metal gate stacks, transistors with 25 nm gate lengths, thin spacers, novel co-implants, advanced activation techniques, extremely thin silicide, and damascene copper contacts.

9:30 a.m.

**27.2 32nm Gate-First High-k/Metal-Gate Technology for High Performance Low Power Applications,** C.H. Diaz, K. Goto, H.T. Huang, Y. Yasuda, C.P. Tsao, T.T. Chu, W.T.Lu, V. Chang, Y.T. Hou, Y.S. Chao, P.F. Hsu, K.C. Lin, C.L. Chen,W.C. Yang, J.A. Ng, C. H. Chen, Y.H. Peng, C.J. Chen, C.C. Chen, M.H. Yu, L.Y. Yeh, K.S. You, K.S. Chen, K.B. Thei, C.H. Lee, S.H. Yang, Y. Ku, J.J. Liaw, K.T. Huang, H. Chuang, M.S. Liang, TSMC

A 32nm high-k metal-gate technology is demonstrated with the highest gate-first performance reported to the best of our knowledge. Drive currents of 1340/940 µmA/µm (n/p) are achieved at $I_{off}$=100 nA/µm, $V_{dd}$=1V, 30nm physical gate length, and 130 nm gate pitch. This technology also provides a high-Vt solution for high-performance low-power applications. Low sub-threshold leakage was achieved while successfully containing $I_{boff}$ and $I_{goff}$ well below 1nA/µm. Ultrahigh-density 0.15$\mu m^2$ SRAM cell is fabricated by high NA 193nm immersion lithography. The technology employs nine levels of Cu interconnect with optimized barrier/Cu deposition. Functional 2Mb SRAM test-chip in 32nm design rule has been demonstrated.

9:55 a.m.

**27.3 32nm General Purpose Bulk CMOS Technology for High Performance Applications at Low Voltage,** F. Arnaud, J. Liu, Y.M. Lee, K.Y. Lim, S. Kohler, J. Chen, B.K. Moon, C.W. Lai, M. Lipinski, L. Sang, F. Guarin, C. Hobbs, P. Ferreira, K. Ohuchi, J. Li, H. Zhuang, P. Mora, Q. Zhang, D.R. Nair, D.H. Lee, K.K. Chan, S. Satadru, S. Yang, J. Koshy, W. Hayter, M. Zaleski, D.V. Coolbaugh, H.W. Kim, Y.C. Ee, J. Sudijono, A. Thean, M. Sherony, S. Samavedam, M. Khare, C. Goldberg, A. Steegen, IBM SRDC

This paper presents a full 32nm CMOS technology using a conventional high-k with single metal gate stack. 22% delay improvement for ring oscillator versus SiON technology, low matching factor and excellent SNM for 0.157$\mu m^2$ SRAM is reported. Hierarchical BEOL based on ELK dielectric is presented. All reliability FEOL criteria have been met.

10:20 a.m.

**27.4 A 45nm Low Power System-On-Chip Technology with Dual Gate (Logic and I/O) High-k/Metal Gate Strained Silicon Transistors,** C.-H. Jan, P. Bai, S. Biswas, M. Buehler, Z.-P. Chen, S. Gannavaram, W. Hafez, J. He, J. Hicks, U. Jalan, N. Lazo, J. Lin, N. Lindert, C. Litteken, M. Jones, M. Kang, K. Komeyli, A. Mezhiba, S. Naskar, S. Olson, J. Park, R. Parker, L. Pei, I. Post, N. Pradhan, C. Prasad, M. Prince, J. Rizk, G. Sacks, H. Tashiro, D. Towner, C. Tsai, Y. Wang, L. Yang, J.-Y. Yeh, J. Yip, K. Mistry, Intel Corporation

A leading edge 45 nm CMOS system-on-chip (SOC) technology using Hafnium-based high-k/metal gate transistors has been optimized for low power products. PMOS/NMOS logic transistor drive currents of 0.86/1.04 mA/µm, respectively, have been achieved at 1.1 V and offstate leakage of 1 nA/µm. HV I/O transistors with robust reliability and other SOC features, including linear resistors, MIS and MIM capacitors, varactors, inductors, vertical BJTs, precision diodes and high density OTP fuses are employed for HV I/O, analog and RF circuit integration.

10:45 a.m.

**27.5 A Low Power 40nm CMOS Technology Featuring Extremely High Density Of Logic (2100kgate/mm$^2$) And SRAM (0.195µm$^2$) For Wide Range Of Mobile Applications With Wireless System,** R. Watanabe, A. Oishi, T. Sanuki, H. Kimijima, K. Okamoto, S. Fujita, H. Fukui, K. Yoshida, H. Otani, E. Morifuji, K. Kojima, M. Inohara, H. Igrashi, K. Honda, H. Yoshimura, T. Nakayama, S. Miyake*, T. Hirai*, T. Iwamoto*, Y. Nakahara*, K. Kinoshita, T. Morimoto, S. Kobayashi, S. Kyoh, M. Ikeda*, K. Imai*, M. Iwai, N. Nakamura*, F. Matsuoka, Toshiba Corporation, *NEC Electronics Corporation

CMOS technology for 40nm low power applications is demonstrated. Gate density of 2100kGate/mm$^2$ and 0.195µm$^2$ SRAM are realized by breaking down conventional trade-off. It results in more than 50% power reduction as a SoC chip by aggressive shrinkage and low voltage operation of RF devices.

11:10 a.m.
**27.6 Gate Length Scaling and High Drive Currents Enabled for High Performance SOI Technology using High-*k*/Metal Gate,** K. Henson, H. Bu, M. H. Na, Y. Liang, U. Kwon, S. Krishnan, J. Schaeffer*, R. Jha, N. Moumen, R. Carter**, C. DeWan, R. Donaton, D. Guo, M. Hargrove**, W. He, R. Mo, R. Ramachandran, K. Ramani**, K. Schonenberg, Y. Tsang**, X. Wang, M. Gribelyuk, W. Yan, J. Shepard, E. Cartier^, M. Frank^, E. Harley, R. Ardnt, R. Knarr, T. Baily, B. Zhang, K. Wong, T. Graves-Abe, E. Luckowski*, D-G. Park^, V. Narayanan^, M. Chudzik, M. Khare, IBM SRDC, *Freescale Semiconductor, **Advanced Micro Devices Inc., ^IBM T.J. Watson Research Center

CMOS devices with high-k/metal gate stacks have been fabricated using a gate-first process flow and conventional stressors at gate lengths of 25nm. AC drive currents of 1630µA/µm and 1190µA/µm have been demonstrated at 1V and 200nA/µm off current for nFETs and pFETs and Tinv of 14 Å…. Devices have been fabricated with Tinv’s down to 12 Å and 10.5 Å demonstrating the scalability of this approach for 32nm and beyond.

11:35 a.m.
**27.7 Implementation and Optimization of Asymmetric Transistors in Advanced SOI CMOS Technologies for High Performance Microprocessors,** J. Hoentschel, A. Wei, M. Wiatr, A. Gehring, T. Scheiper, R. Mulfinger, T. Feudel, T. Lingner, A. Poock, S. Muehle, C. Krueger, T. Hermann*, W. Klix*, R. Stenzel*, R. Stephan, P. Huebler, T. Kammler, P. Shi, M. Raab, D. Greenlaw, M. Horstmann, AMD Fab 36 LLC & Co. KG, *University of Applied Science Dresden

Sub-40nm Lgate asymmetric halo and source/drain extension transistors have been integrated into leading-edge 65nm and 45nm PD-SOI CMOS technologies. The asymmetric NMOS and PMOS saturation drive currents improve up to 12% and 10%, respectively, resulting in performance of NIDSAT=1354µA/µm and PIDSAT=857µA/µm. Product-level implementation show a speed benefit of 12%.

**Session 28: Displays, Sensors, and MEMS - MEMS Actuators and Resonators**
Wednesday, December 17, 9:00 a.m.
Continental Ballroom 1 – 3
Co-Chairs: Joost van Beek, NXP Semiconductors
Koichi Ikeda, Sony Corporation

9:00 a.m.
Introduction
9:05 a.m.
**28.1 Highly Reliable CMOS-Integrated 11mpixel SiGe-Based Micro-Mirror Arrays For High-End Industrial Applications,** L. Haspeslagh, J. De Coster, O. Varela Pedreira, I. De Wolf, B. Du Bois, A. Verbist, R. Van Hoof, M. Willegems, S. Locorotondo, G. Bryce, J. Vaes, B. van Drieenhuizen*, A. Witvrouw, IMEC, *ASML

Very reliable CMOS-integrated 11 MPixel SiGe-based micro-mirror arrays fabricated on top of 6 level metal wafers are reported. The 8µm x 8 µm pixels can be individually addressed by an analog voltage to enable accurate tilt angle modulation. Cupping below 7 nm, RMS roughness below 1 nm and teracycles are demonstrated.

9:30 a.m.
**28.2 Development of Efficient Broadband Digital Acoustic Device Based on Nanocrystalline Silicon Ultrasound Emitter,** N. Koshida, A. Asami, B. Gelloz, Tokyo University of Agriculture and Technology

To make the best use of the characteristics of thermally induced ultrasonic emission from nanocrystalline silicon, a digital drive scheme is introduced into a two-dimensionally arrayed device. Significant output amplitude is observed throughout the frequency of audio to ultrasonic band. This result provides technology platform for digital acoustic applications.

9:55 a.m.
**28.3 Multi-Gate Vibrating-Body Field Effect Transistors (VB-FETs),** D. Grogg, M. Mazza, D. Tsamados, A.M. Ionescu, Ecole Polytechnique Fédérale de Lausanne

We report on the fabrication and characteristics of multi-gate vibrating-body field effect transistors (VB-FETs). Multi-gate VB-FETs with resonance frequencies of 2MHz and 71MHz are demonstrated. The VB-FETs exhibit built-in amplification , low motional resistances and frequency tuning by applied voltages. For the first time, we experimentally demonstrate an active MEM resonator concept, with built-in amplification, which has a negative resistance of -30 Ohms, enabling the possibility to build an oscillator without any sustaining amplifier, thus reducing the power consumption and size. For the first time, we demonstrate a VB-FET mixer-filter based on a single-device operating at 9.84MHz and a VB-FET oscillator at 2.6MHz.

10:20 a.m.
**28.4 A Piezo-Resistive Resonant MEMS Amplifier,** J.T.M. van Beek, K.L. Phan, G.J.A.M. Verheijden, G.E.J. Koops, C. van der Avoort, J. van Wingerden, D. Ernur, J.J.M. Bontemps*, R. Puers**, NXP-TSMC, *Technische Universiteit Eindhoven, **Katholieke Universiteit Leuven

MEMS resonator using electrostatic to piezo-resistive transduction is capable of simultaneous signal filtering and amplification. The mechanical resonance serves as a high Q filter, while the piezo-resistive readout allows for signal amplification. Amplification factors up to 1.7 and Q values up to 60,000 are obtained for a 15 MHz resonator.

10:45 a.m.
**28.5 Exploring the Limits and Practicality of Q-based Temperature Compensation for Silicon Resonators,** J. Salvia, M. Messana, M. Ohline, M.A. Hopcroft*, R. Melamud, S. Chandorkar, H.K. Lee, G. Bahl, B. Murmann, T.W. Kenny, Stanford University, *University of California Berkeley

We investigate quality factor based temperature compensation for micromechanical silicon resonators, including drawbacks and limitations. Our compensated 1.3 MHz prototype oscillator, implemented on a single printed circuit board, achieves temperature stability of ±1 ppm from 0°C to 70°C after multipoint calibration or ±25 ppm after single point calibration.

11:10 a.m.
**28.6 A 145MHz Low Phase-Noise Capacitive Silicon Micromechanical Oscillator,** H.M. Lavasani, A.K. Samarao, G. Casinovi, F. Ayazi, Georgia Institute of Technology

This paper reports a 145MHz low phase-noise capacitive silicon micromechanical oscillator; the highest frequency capacitive micromechanical oscillator reported to-date. The utilized resonator is a high quality-factor (Q~61,000) 145MHz single crystal silicon bulk acoustic resonator, optimized for low motional impedance. The sustaining circuitry is a two-stage amplifier with local shunt-shunt feedback.

11:35 a.m.
**28.7 High Piezoelectric Properties In $LiNbO_3$ Transferred Layer By The Smart Cut$^{TM}$ Technology For Ultra Wide Band BAW Filter Applications,** J.-S. Moulet, M. Pijolat*, J. Dechamp*, F.

Mazen*, A. Tauzin*, F. Rieutord*, A. Reinhardt*, E. Defay*, C. Deguet*, B. Ghyselen, L. Clavelier*, M. Aid*, S. Ballandras**, C. Mazure, SOITEC SA, *CEA-LETI-MINATEC, **Femto ST, UMR CNRS-UFC-ENSMM-UTBM6174

For the first time, HBAR resonators based on monocrystalline films of $LiNbO_3$ fabricated using the Smart Cut™ technology were processed and characterized between 1 and 4 GHz. $k_t^2$ greater than 30% are extracted, by far superior to 7% usually obtained with traditional AlN material. This confirms the interest of this technology for ultra wide band BAW filters.

**Session 29: Modeling and Simulation - Variability Modeling and Technology Optimization**
Wednesday, December 17, 9:00 a.m.
Continental Ballroom 4
Co-Chairs: Gennady Gildenblat, Arizona State University
Wei-Kai Shih, Intel Corporation

9:00 a.m.
Introduction
9:05 a.m.
**29.1 Rapid Design Flows for Advanced Technology Pathfinding (Invited),** P. Christie, A. Nackaerts, A. Kumar*, A. S. Terechko*, G. Doornbos, NXP-TSMC, *NXP Semiconductors

Rapid design flows are presented which enable new device technologies to be assessed at the level of IP blocks with turn-around times of the order of a day. These are applied to the analysis of two competing technologies at the 15nm node and the impact process variations on system level timing at the 45nm node.

9:30 a.m.
**29.2 A Novel, Rigorous Approach To The Dynamic, Large-Signal Stability Analysis Of Semiconductor Devices and Circuits Under Electro-Thermal Interaction,** F. Cappelluti, F.L. Traversa, F. Bonani, G. Ghione, Politecnico di Torino

This paper presents a rigorous numerical approach for studying instabilities in circuits and devices operating under time-periodic conditions. The methodology is entirely developed with the Harmonic Balance technique, with no time-domain calculations involved. As an example of application, the current gain collapse occurring in multifinger AlGaAs/GaAs HBTs is thoroughly studied.

9:55 a.m.
**29.3 Can The Subthreshold Swing In A Classical FET Be Lowered Below 60 Mv/Decade?,** S. Salahuddin, S. Datta, Purdue University

We analyze ferroelectric insulators used as a gate on a classical thermionic type FET and biased in the negative capacitance region, showing that the subthreshold swing in such a transistor can be reduced below the fundamental limit of 60 mV/decade, without reducing ON current, thus effectively overcoming the "Boltzmann tyranny".

10:20 a.m.
**29.4 Sub-20 nm Gate Length FinFET Design: Can High-*k* Spacers Make a Difference?,** A.B. Sachid, R. Francis, M.S. Baghini, D.K. Sharma, K.-H. Bach*, R. Mahnkopf*, V.R. Rao, Indian Institute of Technology Bombay, *Infineon Technologies AG

For 45 nm technology node and below, a sub-20 nm gate length novel device design is proposed to show that high-k spacers in underlap FinFETs (UND-HK-FIN) can significantly improve circuit performance. This is possible as fin thickness can be significantly relaxed in UND-HK-FIN. This is pivotal in improving the performance of circuits. We show that, unlike in planar devices, maximum ION (per electrical width) does not always translate to faster circuits in 3D devices like FinFETs. Instead, this speed comparison in different 3D FinFETs is proposed using ION (per fin).

10:45 a.m.
**29.5 Variability Modeling and Impact on Design (Invited),** H. Onodera, Kyoto University

Measured variabilities from 0.35µm to 90nm processes are explained with a growing concern of within-die components. Variability impact on circuit performance is examined. The effect of layout regularity for mitigating the variability is studied by test structures in a 90nm process and lithography simulation in a 45nm process.

11:10 a.m.
**29.6 Modeling and Analysis of Grain-Orientation Effects in Emerging Metal-Gate Devices and Implications for SRAM Reliability,** H. Dadgour, K. Endo*, V. De**, K. Banerjee, University of California Santa Barbara, *Advanced Industrial Science and Technology, **Intel Corp.

This work introduces an analytical approach to model the random threshold voltage fluctuations in emerging high-k/metal gate devices caused by the dependency of metal work-function on the grain orientations. It is shown that such variations can have significant implications for the performance and reliability of minimum sized circuits such as SRAM cells.

11:35 a.m.
**29.7 Characterization of Metal-Gate FinFET Variability Based on Measurements and Compact Model Analyses,** S. O'uchi, T. Matsukawa, T. Nakagawa, K. Endo, Y.X. Liu, T. Sekigawa, J. Tsukada, Y. Ishikawa, H. Yamauchi, K. Ishii, E. Suzuki, H. Koike, K. Sakamoto, M. Masahara, National Institute of Advanced Industrial Science and Technology

Our FinFET compact model was successfully applied to the characterization of state-of-the-art metal-gate FinFETs. The Vth variation of the transistors was analyzed by combining the transistor size measurement and the model parameter calibration. The extracted variations are incorporated into the compact model and SRAM variability for hp-32-nm node was predicted.

12:00 p.m.
**29.8 Transport-Based Dopant Mapping In Advanced FinFETs,** G.P. Lansbergen, R. Rahman*, C.J. Wellard**, J. Caro, N. Collaert^, S. Biesemans^, G. Klimeck*, L.C.L. Hollenberg**, S. Rogge, Delft University of Technology, *Purdue University, **University of Melbourne, ^IMEC

We present a method to map individual donors in Si FinFETs based on unique features in the current-voltage characteristics attributed to tunneling through individual quantum states. Through careful modeling with multi-million atom simulations, we can identify their chemical species and determine their concentration and depth from the gate interface.

**Session 30: Quantum, Power, and Compound Semiconductors Devices - Heterostructure High-Speed Devices**
Wednesday, December 17, 9:00 a.m.
Continental Ballroom 5
Co-Chairs: Suman Datta, Pennsylvania State University
Rebecca Nicolic, Lawrence Livermore National Laboratory

9:00 a.m.
Introduction
9:05 a.m.
**30.1 30 nm E-mode InAs PHEMTs for THz and Future Logic Applications,** D.-H. Kim, J.A. del Alamo, Massachusetts Institute of Technology

We have demonstrated 30 nm E-mode InAs PHEMTs with outstanding logic performance, scalability, record $f_T$ in E-mode devices, and record combination of $f_T$ and $f_{max}$ above 600 GHz.

9:30 a.m.

**30.2 AlInAs/GaInAs mHEMTs on Silicon Substrates by MOCVD (Invited),** K.M. Lau, C.W. Tang, H. Li, Z. Zhong, Hong Kong University of Science and Technology

Device quality metamorphic $Al_{0.50}In_{0.50}As/Ga_{0.4}7In_{0.53}As$ HEMT structures have been successfully grown by MOCVD on silicon substrates for the first time, with 2-DEG mobilities > 4500 $cm^2$/V-s and sheet carrier densities >7 x 1012 $cm^{-2}$. 1.3- µm gated transistors (Gm = 274mS/mm) demonstrated $f_T$ and $f_{max}$ of 20 and 23GHz, respectively.

9:55 a.m.
**30.3 High-Performance 40nm Gate Length InSb P-Channel Compressively Strained Quantum Well Field Effect Transistors For Low-Power ($V_{CC}$=0.5V) Logic Applications,** M. Radosavljevic, T. Ashley*, A. Andreev*, S.D. Coomber*, G. Dewey, M.T. Emeny*, M. Fearn*, D.G. Hayes*, K.P. Hilton*, M.K. Hudait, R. Jefferies*, T. Martin*, R. Pillarisetty, W. Rachmady, T. Rakshit, S.J. Smith*, M.J. Uren*, D.J. Wallis*, P.J. Wilding*, R. Chau, Intel Corporation, *QinetiQ

We demonstrate for the first time a high-speed and low-power III-V p-channel QWFET using a compressively strained InSb QW structure, which achieves cut-off frequency ($f_T$) of 140GHz at transistor gate length (LG) of 40nm and supply voltage of 0.5V. This represents the highest $f_T$ ever reported for III-V p-channel FETs.

10:20 a.m.
**30.4 SiGe HBT Module with 2.5 ps Gate Delay,** A. Fox, B. Heinemann, R. Barth, D. Bolze, J. Drews, U. Haak, D. Knoll, B. Kuck, R. Kurps, S. Marschmeyer, H.H. Richter, H. Rucker, P. Schley, D. Schmidt, B. Tillack, G. Weidner, C. Wipf, D. Wolansky, Y. Yamamoto, IHP

A novel, double-polysilicon, three-mask SiGe HBT module with selective base epitaxy is presented. By this technology a low-parasitic link between the internal and external base is formed resulting in best-in-class CML ring oscillator gate delays of 2.5ps.

10:45 a.m.
**30.5 Fabrication and Characterisation of Strained Si Heterojunction Bipolar Transistors on Virtual Substrates,** S. Persson, M. Fjer, E. Escobedo-Cousin, G. Malm*, Y.-B. Wang*, P.-E. Hellström*, M. Östling*, E. Parker**, S.H. Olsen and A.G. O'Neill, Newcastle University, *IMIT, KTH, **University of Warwick

Strained Si HBTs have been demonstrated for the first time with maximum current gain of 3700 on a relaxed $Si_{0.85}Ge_{0.15}$ virtual substrate, strained Si emitter and $Si_{0.7}Ge_{0.3}$ base. Pseudomorphic SiGe HBTs and Si control BJTs were also manufactured in parallel having current gains of 334 and 135 respectively.

11:10 a.m.
**30.6 Record PVCR GaAs-based Tunnel Diodes Fabricated on Si Substrates using Aspect Ratio Trapping,** S.L. Rommel, D. Pawlik, P. Thomas, M. Barth, K. Johnson, S.K. Kurinec, Z. Cheng*, J. Li*, J.S. Park*, J. Hydrick*, N. Bai*, M. Carroll*, J. Fiorenza*, A. Lochtefeld*, A. Seabaugh**, Rochester Institute of Technology, *Amberwave Systems Corporation, **University of Notre Dame

Growth of high quality GaAs on Si is produced by Aspect Ratio Trapping followed by metalorganic chemical vapor deposition to grow n+GaAs/n+InGaAs/p+GaAs Esaki interband tunnel diodes. Tunnel diodes fabricated on this material have almost twice the room-temperature peak-to-valley current ratio (PVCR) of the best GaAs diodes ever reported; a PVCR of 46 at room temperature is achieved.

**Session 31: Solid State and Nanoelectronic Devices - Silicon Nanowire Transistors**
Wednesday, December 17, 9:00 a.m.
Continental Ballroom 6
Co-Chairs: Giorgio Baccarani, Università di Bologna
Max Lemme, Harvard University

9:00 a.m.
Introduction
9:05 a.m.
**31.1 Novel Si-Based Nanowire Devices: Will they Serve Ultimate MOSFETs Scaling or Ultimate Hybrid Integration? (Invited),** T. Ernst, L. Duraffourg, C. Dupre, P. Andreucci, A. Hubert, E. Ollier, C. Halte, J. Buckely, O. Thomas, S. Becu, G. Delapierre, G. Molas, V. Nguyen, M. Vinet, M. Colonge, F. Andrieu, T. Poiroux, S. Deleonibus, P. Robert, B. de Salvo, O. Faynot, CEA/LETI MINATEC

9:30 a.m.
**31.2 15nm-Diameter 3D Stacked Nanowires with Independent Gates Operation: ΦFET,** C. Dupre, A. Hubert, S. Becu, M. Jublot, V. Maffini-Alvaro, C. Vizioz, F. Aussenac, C. Arvet**, S. Barnola, J.-M. Hartmann, G. Garnier, F. Allain, J.-P. Colonna, M. Rivoire**, L. Baud, S. Pauliac, V. Loup, P. Rivallin, B. Guillaumot**, G. Ghibaudo*, O. Faynot, T. Ernst, S. Deleonibus, CEA-LETI MINATEC, *IMEP-LAHC, INPG-MINATEC, **STMicroelectronics

For the first time, we report a 3D stacked sub-15nm diameter NanoWire FinFET-like CMOS technology (3D-NWFET) with a new optional independent gate nanowire structure named Î¦FET. Extremely high driving currents for 3D-NWFET (6.5mA/µm for NMOS and 3.3mA/µm for PMOS) are demonstrated thanks to the 3D configuration using a high-k/metal gate stack. We show experimentally that the 3D-NWFET, compared to a co-processed FinFET, relaxes by a factor of 2.5 the channel width requirement for a targeted DIBL and improves transport properties. ΦFET exhibits significant performance boosts compared to Independent-Gate FinFET (IG-FinFET): a 2-decade smaller $I_{OFF}$ current and a lower subthreshold slope (82mV/dec. instead of 95mV/dec.).

9:55 a.m.
**31.3 Experimental Study on Quasi-Ballistic Transport in Silicon Nanowire Transistors and the Impact of Self-Heating Effects,** R. Wang, J. Zhuge, C. Liu, R. Huang, D.-W. Kim*, D. Park*, Y. Wang, Peking University, *Samsung Electronics

The ballistic efficiency and self-heating effects in GAA silicon nanowire transistors (SNWTs) are experimentally investigated. The highest ballistic efficiency is observed in sub-40nm SNWTs at room temperature. However, it is experimentally found that, even if the SNWT is fabricated on bulk-Si substrate, the self-heating effect is worse than SOI devices. The impacts of self-heating on quasi-ballistic SNWTs are discussed as well.

10:20 a.m.
**31.4 Electron Mobility in Multiple Silicon Nanowires GAA nMOSFETs on (110) and (100) SOI at Room and Low Temperature,** J. Chen, T. Saraya, T. Hiramoto, University of Tokyo

Accurate electron mobility in nanowires on (110) SOI have been achieved by split C-V method for the first time. Physical mechanisms that dominate mobility degradation in nanowires have been studied at low temperature. Also, 'double peak' in nanowire mobility at low temperature is observed and investigated.

10:45 a.m.
**31.5 Uniaxial Strain Effects on Silicon Nanowire pMOSFET and Single-Hole Transistor at Room Temperature,** Y.J. Jeong, J. Chen, T. Saraya, T. Hiramoto, University of Tokyo

Uniaxial stress effects on nanowire pMOSFET and single-hole transistor are described. It is found that stress technology is still effective at extremely narrow nanowire pMOSFET but the effects are gradually diminished as NW becomes narrower. In SHT, current modulation, attributed to altered tunneling probability and energy level spacing, is observed.

11:10 a.m.
**31.6 Random Telegraph Noise in N-type and P-type Silicon Nanowire Transistors,** S. Yang, S.D. Suk*, K.-I. Seo*, H. Shin, Seoul National University, *Samsung Electronics Co.

We studied RTN of n-type and p-type silicon nanowire transistors (SNWT) for the first time and derived accurate vertical and lateral trap location equations in nanowire structure. Using the derived equations, accurate trap locations were extracted in the devices with single trap as well as multiple traps.

11:35 a.m.
**31.7 Sub-Femto-Farad Capacitance-Voltage Characteristics of Single Channel Gate-All-Around Nano Wire Transistors for Electrical Characterization of Carrier Transport,** H. Zhao, S.C. Rustagi, N. Singh, F.-J. Ma*, G.S. Samudra*, K.D. Budhaaraju, S.K. Manhas, C.H. Tung, G.Q. Lo, G. Baccarani**, D.L. Kwong, Astar Institute of Microelectronics, *National University of Singapore, **University of Bologna

Measurement of low values of gate capacitance in single channel gate-all-around nanowire transistors is extremely challenging. In this paper, a charge-based capacitance measurement technique is presented to measure this capacitance. Test-keys are designed to enable the I-V measurements from the same test structure and mobility of carriers in the nanowire channels is extracted.

**Session 32: Characterization, Reliability, and Yield - Defect Characterization and Dielectric Breakdown**
Wednesday, December 17, 9:00 a.m.
Continental Ballroom 7 – 9
Co-Chairs: Tanya Nigam, AMD
Zsolt Tokei, IMEC

9:00 a.m.
Introduction
9:05 a.m.
**32.1 Trap Spectroscopy By Charge Injection and Sensing (TSCIS): A Quantitative Electrical Technique For Studying Defects In Dielectric Stacks,** R. Degraeve, M. Cho, B. Govoreanu, B. Kaczer, M.B. Zahid, J. Van Houdt, M. Jurcak, G. Groeseneken, IMEC

Trap Spectroscopy by Charge Injection and Sensing (TSCIS) is proposed as a new, fast and powerful material analysis technique that provides detailed information on the trap density profile and trap energy level in dielectric materials. The principle of the measurement technique is explained and selected results on $SiO_2$, $Si_3N_4$ and $Al_2O_3$ are shown.

9:30 a.m.
**32.2 The Chemistry of Gate Dielectric Breakdown,** X. Li, C.H. Tung*, K.L. Pey, V.L. Lo, Nanyang Technological University, *Institute of Microelectronics

Oxygen vacancy related structural defects are the predominant defect type in the breakdown induced percolation path in ultrathin SiON layer. Oxygen deficiency within the percolation path is radially distributed. The diameter of the path dilates from 30nm to 55nm as the gate leakage current increases from 2μA to 40μA.

9:55 a.m.
**32.3 TDDB in the Presence of Interface States: Implications for the PMOS Reliability Margin,** T. Nigam, P. Peumans, Stanford University

The reduced voltage scaling parameter for PMOS TDDB at low voltages is a concern for ultra-thin gate oxides. We show that this is caused by a change in breakdown statistics due to additional interface defects generated by cold holes. This has implications for product lifetime at low failure fractions and large areas.

10:20 a.m.
**32.4 The Observation of Trapping and Detrapping Effects in High-k Gate Dielectric MOSFETs by a New Gate Current Random Telegraph Noise (IG-RTN) Approach,** C.M. Chang, S.S. Chung, Y.S.

Hsieh*, L.W. Cheng*, C.T. Tsai*, G.H. Ma*, S.C. Chien*, S.W. Sun*, Nationla Chiao Tung Univesity, *United Microelectronics Corporation

A new method, called gate current Random Telegraph Noise (IG RTN), was developed to analyze the quality and reliability of high-k gate dielectric MOSFETs. First, a single electron trapping/detrapping from process induced trap in nMOSFET was observed and its mechanism was also proposed. Secondly, IG RTN has also been successfully applied to detect the different electron tunneling mechanism for a device under high-field or low-field stress. Finally, the soft-breakdown (SBD) behavior of a device can be clearly identified. Its IG RTN characteristic is different from a device before soft-breakdown. It was found that SBD will indeed induce extra leakage current as a result of an additional breakdown path.

10:45 a.m.
**32.5 Breakdown in the Metal/High-k Gate Stack: Identifying the "weak Link" in the Multilayer Dielectric,** G. Bersuker, D. Heh, C. Young, H. Park, P. Khanal, L. Larcher*, A. Padovani**, P. Lenahan^, J. Ryan^, B.H. Lee, H. Tseng, R. Jammy, SEMATECH, *Università di Modena e Reggio Emilia, **Università di Ferrara, ^Pennsylvania State University

We apply a systematic approach to identify a high-k/metal gate stack degradation mechanism. Our results demonstrate that the interfacial layer is the major factor controlling the overall degradation and breakdown of the gate stacks in inversion. Defects contributing to the gate stack degradation are associated with the high-k/metal -induced oxygen vacancies in the interfacial layer.

**Session 33: Memory Technology - DRAM and NOR Flash Memory**
Wednesday, December 17, 9:00 a.m.
Imperial Ballroom
Co-Chairs: Hideaki Aochi, Toshiba Corporation
Adrian Ionescu, Ecolé Polytechnique Fédérale de Lausanne

9:00 a.m.
Introduction
9:05 a.m.
**33.1 55 nm Capacitor-less 1T DRAM Cell Transistor with Non-Overlap Structure,** K.-W. Song, H. Jeong, J.-W. Lee, S.I. Hong, N.-K. Tak, Y.-T. Kim, Y.L. Choi, H.S. Joo, S.H. Kim, H.J. Song, Y.C. Oh, W.-S. Kim, Y.-T. Lee, K. Oh, C. Kim, Samsung Electronics Co.

This paper presents a capacitor-less 1T DRAM cell transistor with high scalability and long retention time. It adopts gate to source/drain non-overlap structure to suppress junction leakage, which results in 80ms retention time at 85ºC with gate length of 55nm. Compared to the previous reports, proposed cell transistor shows twice longer retention time even though the gate length shrinks to the half of them. By TCAD analysis, we have confirmed that the improvements are attributed to the superiority of the proposed device structure.

9:30 a.m.
**33.2 Autonomous Refresh of Floating Body Cell (FBC),** T. Ohsawa, R. Fukuda, T. Higashi*, K. Fujita, F. Matsuoka, T. Shino, H. Furuhashi, Y. Minami, H. Nakajima, T. Hamamoto, Y. Watanabe, A. Nitayama, T. Furuyama, Toshiba Corporation, *Toshiba Microelectronics Corp.

Physics of autonomous refresh of FBC is presented. Current input by impact ionization to the body is balanced with output by charge pumping. 500 µA retention current for 1Gbit memory is achieved in 32nm with 4ms retention. If gate direct tunneling current is used for output, FBC can realize static RAM.

9:55 a.m.
**33.3 Evaluation of 1T RAM using Various Operation Methods with SOONO (Silicon-On-Ono) Device,** H.J. Bae, H.J. Song, Y.L. Choi, S.H. Kim, S.I. Hong, C. W. Oh, D.-W. Kim, G. Jin, K.S. Oh, W.-S. Lee, Samsung Electronics Co.

We demonstrated 1T RAM without capacitor with various operation method using SOONO (Silicon-On-ONO) devices. The bipolar junction transistor (BJT) operation method shows better current sensing margin between state “1” and “0” comparing to that of impact ionization method. Current sensing margin of 39 µA with 58 ms of hold time at LG = 51 nm under 358 K is achieved by applying the BJT operation, which is the best characteristics of retention and sensing margin ever reported as 1T RAM. In addition, a memory effect and retention characteristics with LG = 40 nm SOONO device also observed. From these results, the BJT operation method offers the possibility of 1T RAM as stand alone device.

10:20 a.m.
**33.4 A 6F$^2$ Buried Wordline DRAM Cell for 40nm and Beyond,** T. Schloesser, F. Jakubowski, J. v. Kluge, A. Graham, S. Slesazeck, M. Popp, P. Baars, K. Muemmler, P. Moll, K. Wilson, A. Buerke, D. Koehler, J. Radecker, E. Erben, U. Zimmermann, T. Vorrath, B. Fischer*, G. Aichmayr, R. Agaiby, W. Pamler*, T. Schuster, W. Bergner, W. Mueller, Qimonda Dresden GmbH & Co., *Qimonda AG

We present a 46nm 6F$^2$ buried wordline (bWL) DRAM technology, enabling the smallest cell size of 0.013µm$^2$ published to date. We demonstrate high array device on-current, small parameter variability, high reliability and small parasitic capacitances, resulting in an excellent array performance. The array device can be scaled down to 30nm without compromising its performance.

10:45 a.m.
**33.5 Stackable Memory of 3D Chip Integration for Mobile Applications (Invited),** S.Q. Gu, F. Wang, M. Suh, D. Lisk, M. Nowak, Qualcomm Incorporated

11:10 a.m.
**33.6 A Highly Punchthrough-Immune Operation Method For An Ultra-Short-Channel Hot-Carrier-Injection Type Non-Volatile Memory Cell,** W.-J. Tsai, T.F. Ou, J.S. Huang, C.H. Cheng, C.-Y. Lu, T. Wang, K.F. Chen, T.T. Han, T.C. Lu, K.C. Chen, C.-Y. Lu, Macronix International

A novel bias scheme is proposed for non-volatile memory cells arranged in a virtual-ground array that utilizes hot-carrier injections for program and erase operations. By taking two adjacent cells on the same wordline as a unit, and letting the commonly shared n+ region being floating during program and erase, punchthrough immunity is greatly improved. Program/erase speed, endurance, and retention characteristics are comparable to conventional operations. NBit cell is projected to be workable at sub-40nm node by such scheme.

11:35 a.m.
**33.7 Performance and Reliability of a 4MB Si Nanocrystal NOR Flash Memory with Optimized 1T Memory Cells,** C. Gerardi, G. Molas*, G. Albini, E. Tripiciano, M. Gely*, A. Emmi, O. Fiore, E. Nowak*, D. Mello, M. Vecchio, L. Masarotto*, R. Portoghese, P. Scheiblin*, B. De Salvo*, S. Deleonibus*, A. Maurelli, STMicroelectronics, *CEA-LETI

We integrate Silicon nanocrystals in a 4Mb NOR-Flash array (90nm node). Main original improvements are cylindrical symmetry of 1T bit-cells and optimized ONO dielectric. Memory characteristics are improved and parasitic charge trapping is reduced, resulting in excellent performance and reliability, clearly demonstrating the high potential for future embedded applications.

**Session 34: Memory Technology - Nanoscale Poly-FG and Charge Trap Flash Non-Volatile Memories**
Wednesday, December 17, 1:30 p.m.
Grand Ballroom A
Co-Chairs: Tejas Krishnamohan, Intel Corporation
Jong-Ho Lee, Kyungpook National University

1:30 p.m.
Introduction
1:35 p.m.

**34.1 Floating Gate Super Multi Level NAND Flash Memory Technology for 30nm and Beyond,** T. Kamigaichi, F. Arai, H. Nitsuta, M. Endo, T. Murata, H. Takekida, T. Izumi, K. Uchida, T. Maruyama, I. Kawabata, Y. Suyama, A. Sato, K. Ueno, H. Takeshita, Y. Joko, S. Watanabe, Y. Liu, H. Meguro, A. Kajita, Y. Ozawa, and T. Watanabe, S. Sato*, H. Tomiie*, Y. Kanamaru*, R. Shoji*, C.H. Lai*, M. Nakamichi*, K. Oowada*, T. Ishigaki*, G. Hemink*, D. Dutta*, Y. Dong*, C. Chen*, G. Liang*, M. Higashitani*, J. Lutze*, Toshiba Corporation, *SanDisk Corporation

Floating Gate NAND Flash Memory Technology for 30nm and beyond has been successfully developed. Wide program/erase window, tight natural Vth distribution, and good cell reliabilities such as program disturb, rogram/erase endurance and data retention are successfully demonstrated, which are essential to realize Super MLC.

2:00 p.m.
**34.2 Novel Model For Cell - System Interaction (MCSI) In NAND Flash,** C. Friederich, J. Hayek, A. Kux, T. Müller**, N. Chan**, G. Koebernik, M. Specht, D. Richter, D. Schmitt-Landsiedel*, Qimonda Flash GmbH, *Technical University Munich, **Qimonda Dresden GmbH & Co.

For the first time a stochastic model of the program operation in NAND Flash memories is proposed. The model incorporates intrinsic noise effects on the cells' threshold voltage ($V_{th}$) distribution in incremental step pulse programming (ISPP) schemes. An excellent match with experimental data at 48 nm ground rule is shown.

2:25 p.m.
**34.3 Scaling Trends For Random Telegraph Noise In Deca-Nanometer Flash Memories,** A. Ghetti, C. Monzio Compagnoni*, F. Biancardi*, A.L. Lacaita*, S. Beltrami, L. Chiavarone, A.S. Spinelli*, A. Visconti, Numonyx R&D, *Politecnico di Milano

In this work we present a thorough investigation of RTN scaling trends for both NAND and NOR Flash memories, including experimental and modeling results. A comprehensive analysis of RTN dependence on cell parameters is presented. Results are of utmost importance to derive RTN design margins in next generation technology nodes

2:50 p.m.
**34.4 10 nm Bulk-Planar SONOS-type Memory with Double Tunnel Junction and Sub-10 nm Scaling Utilizing Source to Drain Direct Tunnel Sub-threshold,** R. Ohba, Y. Mitani, N. Sugiyama, S. Fujita, Toshiba Corporation

10nm SONOS-type device with double tunnel junction, where Si nanocrystals are lying between double tunnel oxides, shows an excellent non-volatility in low w/e voltages. 8nm double junction SONOS shows a reliable performance by realizing S/D direct tunnel sub-threshold. Further device scaling and improvement are possible utilizing S/D direct tunnel sub-threshold. Double junction SONOS is a promising candidate in sub-10nm region.

3:15 p.m.
**34.5 Good 150°C Retention and Fast Erase Charge-Trapping-Engineered Memory with Scaled $Si_3N_4$,** S.H. Lin, A. Chin*, F.S. Yeh, S.P. McAlister**, National Tsing-Hua University, *National Chiao-Tung University, **National Research Council of Canada

At 150ºC under fast 100µs and 16V P/E, the charge-tapping-engineered memory with very thin 5nm $Si_3N_4$ shows good device integrity of large initial 5.6V and 3.8V 10-year extrapolated retention. These are much better than the initial 3.3V and 1.7V 10-year data for similar structure without extra 0.9nm EOT deep-trapping HfON.

3:40 p.m.
**34.6 Sub-50nm DG-TFT-SONOS - The Ideal Flash Memory for Monolithic 3-D Integration,** A.J. Walker, Schiltron Corporation

A revolutionary 3-D stackable sub-50nm double-gate TFT SONOS technology is reported with strings of up to 64 cells consisting of the smallest TFT's to date. Read- and program-pass disturbs have been extinguished. Excellent endurance and retention are shown. Monolithic 3-D integration is ensured through ~zero S/D diffusion.

4:05 p.m.
**34.7 Disturbless Flash Memory Due to High Boost Efficiency on BiCS Structure and Optimal Memory Film Stack for Ultra High Density Storage Device,** Y. Komori, M. Kido, M. Kito, R. Katsumata, Y. Fukuzumi, H. Tanaka, Y. Nagata*, M. Ishiduki, H. Aochi, A. Nitayama, Toshiba Corporation, *Toshiba Information Systems Corporation

Program and erase operation on NAND-string of Bit-Cost Scalable (BiCS) flash memory has been successfully achieved. High boost efficiency of floating pillars and ONON (block oxide/charge SiN/tunnel oxide/tunnel SiN) structure as a memory film stack improve disturbance characteristics low enough to realize tera-bit density of three dimensional flash memory.

**Session 35: CMOS Devices and Technology - Alternative MOSFET Device Architectures and Materials**
Wednesday, December 17, 1:30 p.m.
Grand Ballroom B
Co-Chairs: Raphael Clerc, IMEP
Kiyotaka Imai, NEC Electronics Corporation

1:30 p.m.
Introduction
1:35 p.m.
**35.1 Enhancing SRAM Cell Performance by Using Independent Double-Gate FinFET,** K. Endo, S.-I. O'uchi, Y. Ishikawa, Y. Liu, T. Matsukawa, K. Sakamoto, J. Tsukada, K. Ishii, H. Yamauchi, E. Suzuki, M. Masahara, National Institute of Advanced Industrial Science and Technology

SRAM cells with Vth-controllable independent double-gate (IDG) FinFETs have been fabricated. The performance of the SRAM cell with various circuit topologies has been investigated comprehensively. Both a reduction of leakage current and an enhancement of noise margins have been successfully demonstrated by introducing the IDG FinFETs into the SRAM cells.

2:00 p.m.
**35.2 Full-Field EUV and Immersion Lithography Integration in 0.186μm$^2$ FinFET 6T-SRAM Cell,** A. Veloso, S. Demuynck, M. Ercken, A.M. Goethals, M. Demand, J.-F. de Marneffe, E. Altamirano, A. De Keersgieter, C. Delvaux, J. De Backer, S. Brus, J. Hermans, B. Baudemprez, F. Van Roey, G.F. Lorusso, C. Baerts, D. Goossens, C. Vrancken, S. Mertens, J.J. Versluijs, V. Truffert, C. Huffman, D. Laidler, N. Heylen, P. Ong, B. Parvais, M. Rakowski, S. Verhaegen, A. Hikavyy, H. Meiling*, B. Hultermans*, L. Romijn*, C. Pigneret*, S. Lok*, A. Van Dijk*, K. Shah**, A. Noori**, J. Gelatos**, R. Arghavani**, R. Schreutelkamp**, P. Boelen**, O. Richard, H. Bender, L. Witters, N. Collaert, R. Rooyackers, P. Absil, A. Lauwers, M. Jurczak, T. Hoffmann, S. Vanhaelemeersch, R. Cartuyvels, K. Ronse, S. Biesemans, IMEC, *ASML, **Applied Materials

We report major advancement in full-field EUV Lithography technology, using it for single patterning of contact level of 0.186μm$^2$ 6T-SRAMs, with good overlay values and W contacts. Other key features: high-k/Metal Gate FinFETs with good CD control, ultra-thin NiPt-silicide, spacers without Si recess at dense pitches. Good SRAM scalability and healthy electrical characteristics for cell transistors are obtained.

2:25 p.m.
**35.3 Electron Transport in Gate-All-Around Uniaxial Tensile Strained-Si Nanowire n-MOSFETs,** P. Hashemi, L. Gomez, M. Canonico*, J.L. Hoyt, Massachusetts Institute of Technology, *Freescale Semiconductor Inc.

The intrinsic performance and electron mobility of uniaxially-tensile strained-Si (~2.1GPa) Gate-All-Around (GAA) nanowire n-MOSFETs fabricated by a top-down approach are investigated, for the first time. GAA strained-Si devices with width ~7-49nm and thickness ~6-9nm show ideal subthreshold swing and ~2X drive current, mobility and transconductance enhancement over Si GAA nanowires.

2:50 p.m.
**35.4 Nanowire FETs for Low Power CMOS Applications Featuring Novel Gate-All-Around Single Metal FUSI Gates with Dual $\Phi_m$ and $V_T$ Tune-Ability,** Y. Jiang, T.Y. Liow, N. Singh, L.H. Tan, G.Q. Lo, D.S.H. Chan*, D.L. Kwong, Institute of Microelectronics, *National University of Singapore

A simple and cost-effective single metal gate scheme was successfully demonstrated to form gate-all-around (GAA) nanowire FETs with optimized dual $V_T$ for low power CMOS applications. FUSI gate-induced stress effects were shown to be of great relevance to device performance. At an $I_{Off}$ of 20 pA/µm, superior $I_{On}$ of 1180 and 405 µA/µm were obtained at a $V_{DD}$ of 1.2 V, exceeding other benchmark LSTP work.

3:10 p.m.
**35.5 Record $I_{on}/I_{off}$ Performance Ffor 65nm Ge PMOSFET And Novel Si Passivation Scheme For Improved EOT Scalability,** J. Mitard, B. De Jaeger, F.E. Leys, G. Hellings, K. Martens, G. Eneman, D.P. Brunco*, R. Loo, D. Shamiryan, T. Vandeweyer, G. Winderickx, E. Vrancken, K. De Meyer, M. Caymax, L. Pantisano, M. Meuris, M.M. Heyns, IMEC, *Intel

We report on a 65nm Ge pFET with a record performance of Ion = 478µA/µm and $I_{off,s}$= 37nA/µm @$V_{dd}$= -1V. These improvements are quantified and understood with respect to halo/extension implants, minimizing series resistance and gate stack engineering. A better control of Ge in-diffusion using a low-temperature Epi-silicon passivation process allows achieving 1nm EOT Ge-pFET with increased performance.

3:35 p.m.
**35.6 Interface-Controlled Self-Align Source/Drain Ge PMOSFETS Using Thermally-Oxidized $GeO_2$ Interfacial Layers,** Y. Nakakita, R. Nakane, T. Sasada, H. Matsubara, M. Takenaka, S.-N. Takagi, The Univesity of Tokyo

The examination and the understanding of $GeO_2$/Ge interfaces and the inversion-layer mobility are quite important, so Ge pMOSFETs with the thermally-grown pure $GeO_2$/Ge interfaces have been successfully demonstrated by using Al gate first processes. Hole mobility enhancement against the Si universal one has been obtained with the SiO/ $GeO_2$/Ge gate stack.

**Session 36: Modeling and Simulation - Enhanced Mobility and III-V Devices**
Wednesday, December 17, 1:30 p.m.
Continental Ballroom 4
Co-Chairs: Massimo Fischetti, University of Massachusetts
Phil Oldiges, IBM

1:30 p.m.
Introduction
1:35 p.m.
**36.1 Physics-Based Compact Model of III-V Heterostructure FETs for Digital Logic Applications,** S. Oh , H.-S.P. Wong, Stanford University

A physics-based analytical compact model of InGaAs FETs for logic applications is developed which neither heavily depend on parameter extraction nor require any time-consuming computation, enabling digital circuit design and circuit-level performance estimation for III-V FETs. The model captures SCE, trapezoidal well QW energies and capacitance including potential profile information.

2:00 p.m.
**36.2 Full-Band and Atomistic Simulation of Realistic 40 nm InAs HEMT,** M. Luisier, N. Neophytou, N. Kharche, G. Klimeck, Purdue University

In this paper we present a highly-efficient ballistic, two-dimensional, full-band, atomistic, and quantum mechanical simulator to study realistic InAs HETMs with InGaAs barriers . The tool is based on the sp3d5s* tight-binding model and a Wave Function approach, equivalent to the Non-Equilibrium Green's Function formalism. It allows the simulation of 140 nm long devices with a channel thickness up to 12 nm. Quantitative agreement with experimental data is demonstrated.

2:25 p.m.
**36.3 NEGF Analysis of InGaAs Schottky Barrier Double Gate MOSFETs,** H.S. Pal, T. Low, M.S. Lundstrom, Purdue University

A study of InGaAs Schottky barrier FET is conducted from a structural and material perspective by comparing it with InGaAs MOSFET and Si SBFET counterpart. Device metric, i.e. subthreshold swing and gate transconductance, are systematically evaluated. We demonstrate that InGaAs SBFET should perform better than MOSFET counterpart as a high performance device.

2:50 p.m.
**36.4 Deterministic Multisubband Device Simulations For Strained Double Gate PMOSFETS Including Magnetotransport,** A.-T. Pham, C. Jungemann*, B. Meinerzhagen, Technological University Braunschweig, *Bundeswihr University

The authors present, for the first time, 2D deterministic multisubband device simulations based on the self consistent solution of SE-PE-BTE for PMOSFETs without any simplification of the subband structure. The magnetotransport is included. The magnetoresistance mobility extraction is shown to be better than the conventional mobility extraction technique.

3:15 p.m.
**36.5 Comparison of (001), (110) and (111) Uniaxial- and Biaxial- Strained-Ge and Strained-Si PMOS DG FETs for ALL Channel Orientations: Mobility Enhancement, Drive Current, Delay and Off-State Leakage,** T. Krishnamohan, D. Kim, T.V. Dinh*, A.-T. Pham**, B. Meinerzhagen**, C. Jungemann*, K. Saraswat, Stanford University, *University of Armed Forces, **Technological University of Braunschweig

Through detailed simulations we have thoroughly compared the performance in highly scaled, strained-Ge and strained-Si PMOS DG FETs for all three surface orientations (001), (110) and (1110). We have examined all channel orientations, and benchmarked the mobility enhancement, high-field velocity, drive current, delay and off-state leakage.

3:40 p.m.
**36.6 On Strain And Scattering In Deeply-Scaled N-Channel MOSFETS: A Quantum-Corrected Semiclassical Monte Carlo Analysis,** N. Shi, L.F. Register, S.K. Banerjee, The University of Texas at Austin

In this work we examine the role of scattering and mobility in the analysis of short channel unstrained and strained MOSFETs, and find perhaps unexpected benefits and limitations of strain, as well as limitations on the use of mobility for predicting these.

**Session 37: Process Technology - Advanced Source-Drain Engineering and Memory Processing**
Wednesday, December 17, 1:30 p.m.
Imperial Ballroom
Co-Chairs: Hsing-Huang Tseng, SEMATECH
Xiaomang Chen, IBM

1:30 p.m.

Introduction

1:35 p.m.

**37.1 Aggressive Design of Millisecond Annealing Junctions for Near-Scaling-Limit Bulk CMOS using Raised Source/Drain Extensions,** K. Yako, K. Uejima, T. Yamamoto, A. Mineji*, T. Nagumo, T. Ikezawa**, N. Matsuzaka*, S. Shishiguchi*, T. Hase, M. Hane, LSI Fundamental Research Lab., *NEC Electronics Corp., **NEC Informatec Systems Ltd.

An aggressive junction design concept is proposed for further scaling of bulk CMOS featuring selective epi-growth raised source/drain extensions in conjunction with high temperature millisecond annealing process. The junction design window enlarged by introducing the RSDext enables us to perform elaborate control of slight “intentional” diffusion onto the MSA process rather than aiming complete-diffusion-less junctions. Such the “effective” ultra-shallow junctions under the raised S/D-extensions are demonstrated, in this paper, to exhibit both lower parasitic resistance and lower junction leakage while maintaining superior short-channel-effect suppression, i.e. $V_{th}$ roll-off characteristics, and any reliability issues.

2:00 p.m.

**37.2 Effective Reduction of Threshold Voltage Variability and Standby Leakage using Advanced Co-implantation and Laser Anneal for Low Power Applications,** H. Lee, H.-S. Rhee, M.-S. Kim, H.-S. Chung, S.-M. Lim, M.-H. Park, N.-I. Lee, J.S. Yoon, Samsung Electronics Co.

We have successfully reduced threshold voltage variation by combination of co-implantation and laser spike anneal on 45nm low power SoC platform even without introducing high-K gate stack. The systematic junction profile design for n- and pFET enables us to reduce random dopant variation significantly without compromising standby leakage, drive current and gate oxide integrity, which finally contributes to RO ~5% performance improvement at equivalent Iddq and ensures high yield of SRAM array by reducing beta and gamma ratio variation.

2:25 p.m.

**37.3 Conformal Doping for FinFETs and Precise Controllable Shallow Doping for Planar FET Manufacturing by a Novel $B_2H_6$/Helium Self-Regulatory Plasma Doping Process,** Y. Sasaki, K. Okashita, K. Nakamoto, T. Kitaoka, B. Mizuno, M. Ogura*, Ultimate Junction Technologies Inc., *Matsushita Electric Industrial Co. Ltd.

The new SRPD has provided desirable conformal doping layer for extension of FinFETs. The precise process controllability of ultra-shallow doping for planar FETs has been also successfully realized. It is sure that this new SRPD is mandatory for both FinFETs and planar FETs for 32nm and beyond.

2:50 p.m.

**37.4 Contact Resistance Reduction Of Pt-Incorporated NiSi For Continuous CMOS Scaling ~ Atomic Level Analysis Of Pt/B/As Distribution Within Silicide Films ~,** T. Sonehara , A. Hokazono , H. Akutsu , T. Sasaki*, H. Uchida*, M. Tomita , H. Tsujii , S. Kawanaka , S. Inaba, Y. Toyoshima, Toshiba Corporation, *Toshiba Nanoanalysis Corporation

Atom distributions both at silicide/Si interface and at silicide grain boundary in $Ni_{1-x}Pt_xSi$ films are investigated by Atomic level analysis. The role of Pt in $Ni_{1-x}Pt_xSi$ films is discussed and the model of Rc reduction for n and pMOS is proposed based on the electrical and analytical results.

3:15 p.m.

**37.5 Band Engineered Charge Trap NAND Flash with Sub-40nm Process Technologies (Invited),** S. Choi, S.J. Baik, J.-T. Moon, Samsung Electronics, Co.

3:40 p.m.

**37.6 0.5 nm EOT Low Leakage ALD $SrTio_3$ On TiN MIM Capacitors For DRAM Applications,** N. Menou, X.P. Wang, B. Kaczer, W. Polspoel, M. Popovici, K. Opsomer, M.A. Pawlak, W. Knaepen*, C. Detavernier*, T. Blomberg**, D. Pierreux^, J. Swerts^, J.W. Maes^, P. Favia, H. Bender, B. Brijs, W.

Vandervorst, S. Van Elshocht, D.J. Wouters, S. Biesemans, J.A. Kittl, IMEC, *Gent University, **ASM Microchemistry, ^ASM Belgium

We demonstrate record low leakage-EOT ($3.5x10^{-7}$ $A/cm^2$ at 1V, EOT=0.49 nm) MIM capacitors fabricated using low temperature (250ºC) ALD $SrTiO_3$ on ALD TiN bottom electrodes. $Sr(t\text{-}Bu_3Cp)_2$, $H_2O$, $Ti(OCH_3)_4$ precursors, optimized composition (Sr-rich) and process conditions allowed minimization of interfacial EOT penalties and leakage, enabling STO on TiN.