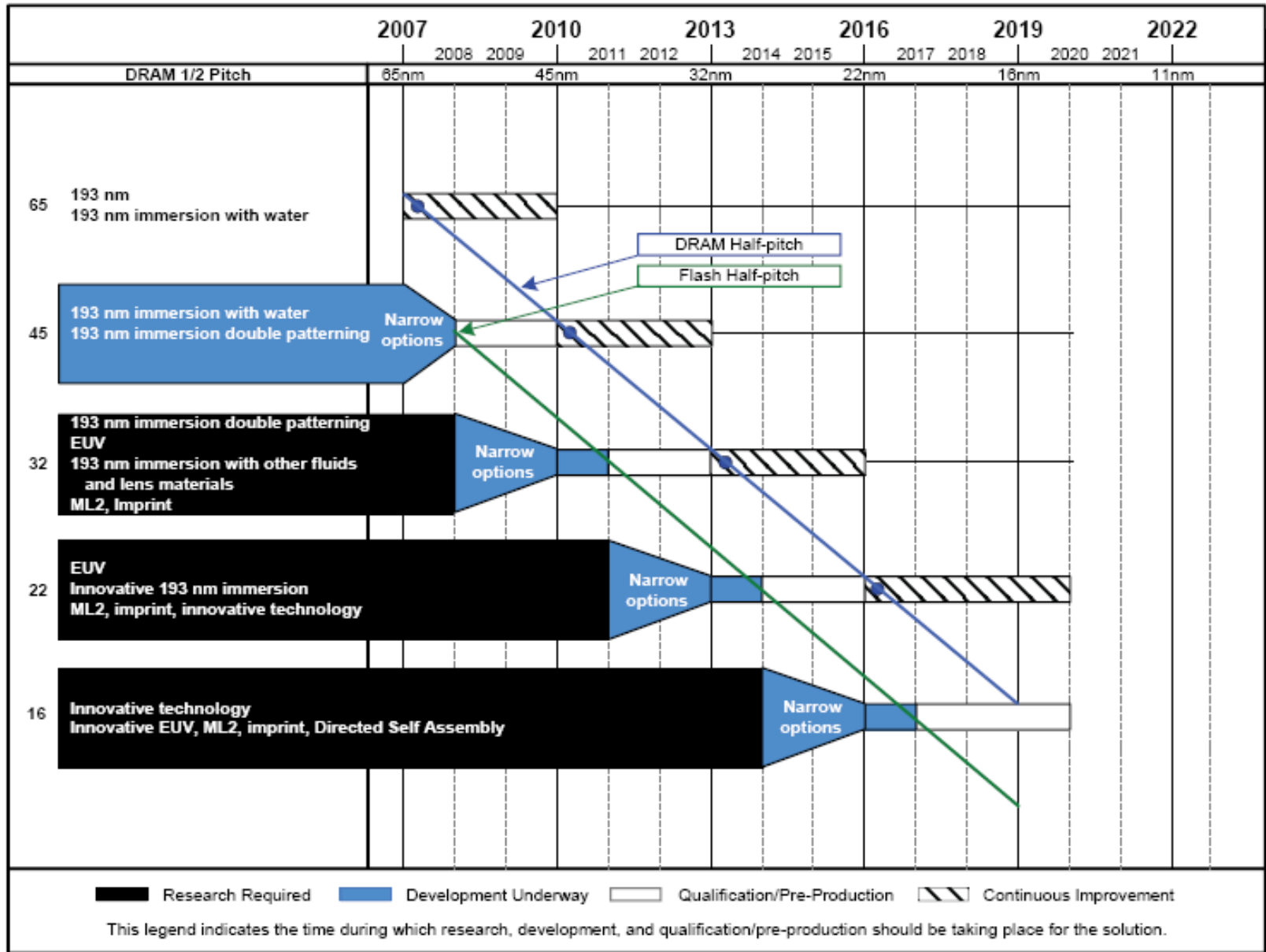




2008 Litho ITRS

Lithography iTWG - Meeting
July 2008

Litho Potential Solutions



Potential Show Stoppers

- Resist Limits (Shot Noise, Photo electron Blur)
- Cost of Ownership – all technologies
- EUV Lithography
 - Source availability at needed powers and life
 - Extendibility
 - Mask Defects

Conclusions

- Update Lithographic Requirements
 - Separate into DRAM, Flash, MPU
- Double patterning
 - 3 types
 - Double Patterning Spacer Technology
 - DP/DE Uncorrelated Lines / Correlated Lines

Litho Requirements

Table 76a&b Lithography Technology Requirements—Near-term Years

Year of Production	2007	2008	2009	2010	2011	2012	2013
DRAM ½ pitch (nm) (contacted)	68	59	52	45	40	36	32
DRAM							
DRAM ½ pitch (nm)	68	59	52	45	40	36	32
CD control (3 sigma) (nm) [B]	7.1	6.2	5.4	4.7	4.2	3.7	3.3
Contact in resist (nm)	75	65	57	50	44	39	35
Contact after etch (nm)	68	59	52	45	40	36	32
Overlay [A] (3 sigma) (nm)	13.6	11.9	10.3	9.0	8.0	7.1	6.4
Flash							
Flash ½ pitch (nm) (un-contacted poly)	54	45	40	36	32	28	25
CD control (3 sigma) (nm) [B]	5.6	4.7	4.2	3.7	3.3	2.9	2.6
Contact in resist (nm)	59	49	44	39	35	31	28
Contact after etch (nm)	54	45	40	36	32	28	25
Overlay [A] (3 sigma) (nm)	17.7	14.8	13.2	11.8	10.5	9.4	8.3
MPU							
MPU/ASIC Metal 1 (M1) ½ pitch (nm)	68	59	52	45	40	36	32
MPU gate in resist (nm)	54	47	41	35	31	28	25
MPU physical gate length (nm) *	32	29	27	24	22	20	18
Gate CD control (3 sigma) (nm) [B] **	3.3	3.0	2.8	2.5	2.3	2.1	1.9
Contact in resist (nm)	84	73	64	56	50	44	39
Contact after etch (nm)	77	67	58	51	45	40	36
Overlay [A] (3 sigma) (nm)	17	15	13	11	10.0	8.9	8.0

Double patterning table	2007	2008	2010	2013	2016
NAND FLASH [DRAM] HP (nm)	54 [65]	45 [57]	36 [45]	25 [32]	18 [22]
Image placement for double patterning	4.9	4.4	3.4	2.4	1.9
Difference in CD Mean-to-target for two masks as a double patterning set	2.6	2.3	1.8	1.3	1.0
<i>Dual line: mask image placement</i>	1.9	1.7	1.3	0.90	0.60
<i>Dual line: mask CD range</i>	1.9	1.7	1.3	0.90	0.60
<i>Dual space: repeatability and uniformity of etch bias for double patterning</i>	1.2	1.0	0.80	0.60	0.40
Double patterning: requirement for printed features					
<i>Spacer PEE process: nominal duty cycle required for printed features</i>	1:3	1:3	1:3	1:3	1:3
<i>Spacer PEE process: first pass CD control (after etch)</i>	4.6	3.9	3.0	2.1	1.6
<i>Spacer PEE process: thickness deviation of final layer</i>	1.1	0.90	0.70	0.55	0.35
<i>Spacer PEE process: thickness uniformity of final layer</i>	2.2	1.8	1.4	1.1	0.70
<i>Spacer PEE: sidewall angle of printed features</i>	To be filled by US TWG or discussed in San Francisco				
<i>Spacer PEE: repeatability and uniformity of etch bias (per pass; 2 more passes required)</i>	1.2	1.0	0.80	0.60	0.40