



Improving System Performance and Longevity with a New NAND Flash Architecture

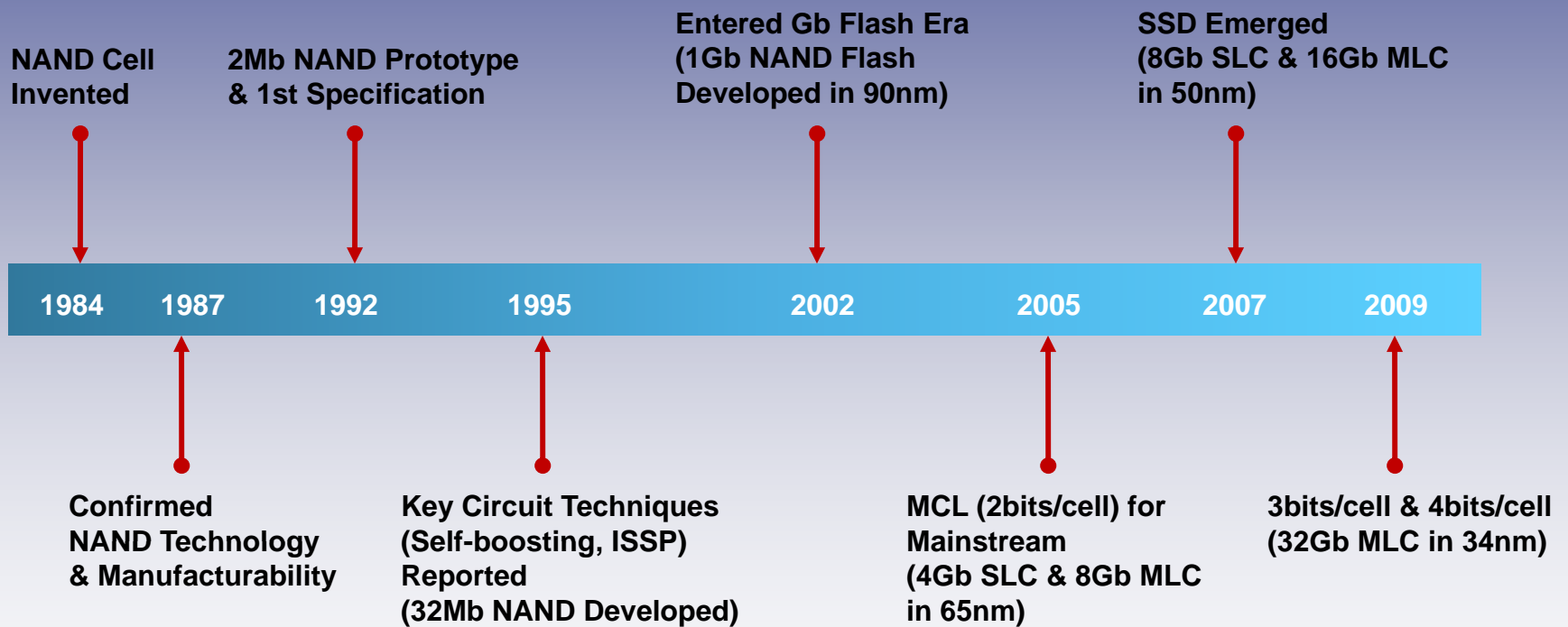
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Vice President, Research & Development
MOSAID Technologies Inc.



Agenda

- Background
- Technical Innovations
- Solutions for Emerging Applications
- Summary

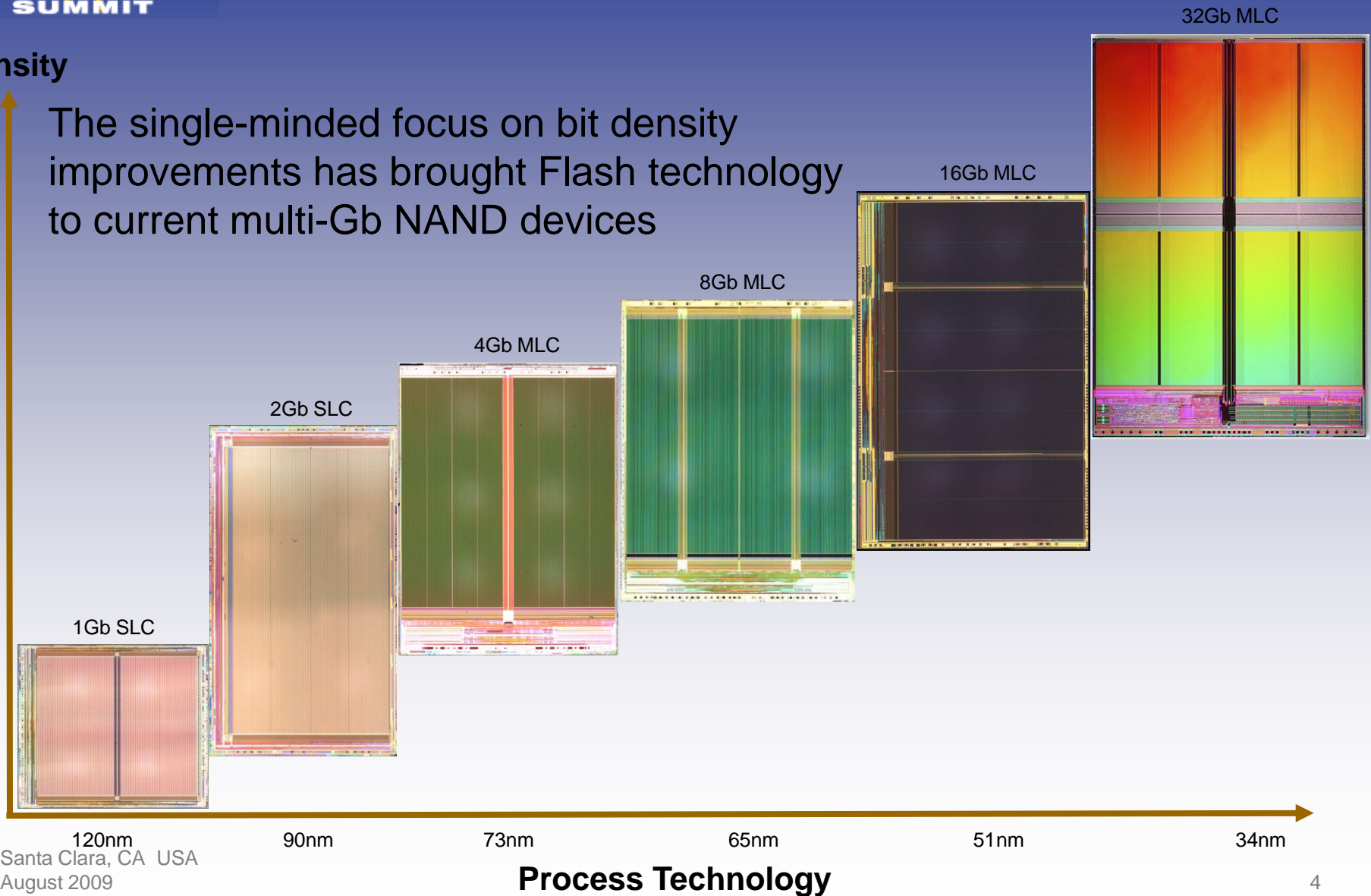
NAND Technology Timeline



NAND Flash Progression

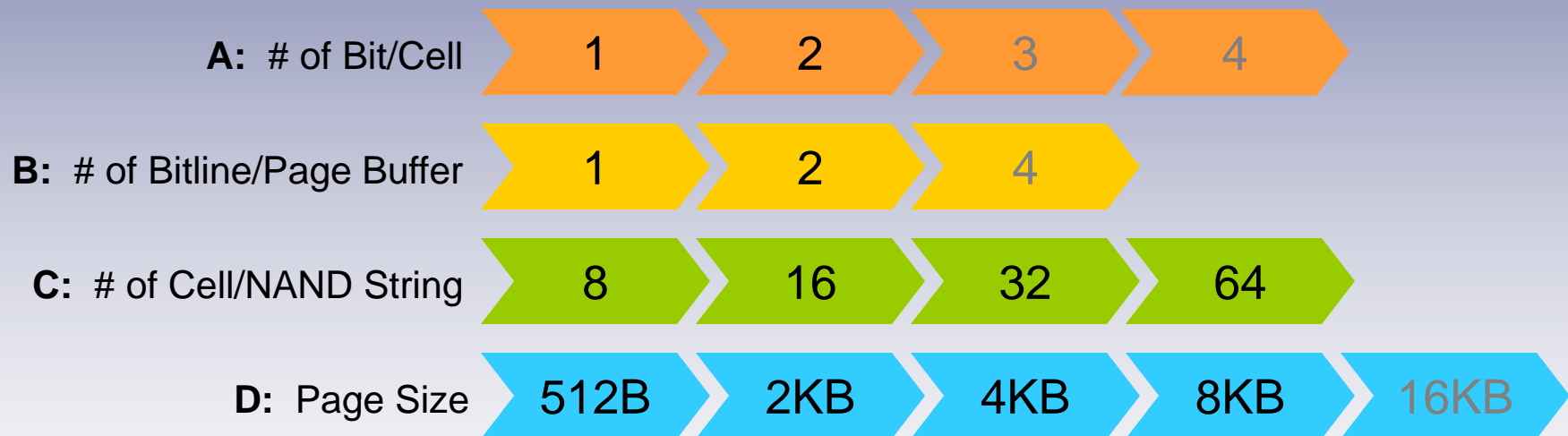
Density

The single-minded focus on bit density improvements has brought Flash technology to current multi-Gb NAND devices



NAND Architecture Trend

- Primary focus is density for cost and market adoption
- Page-based program and block-based erase

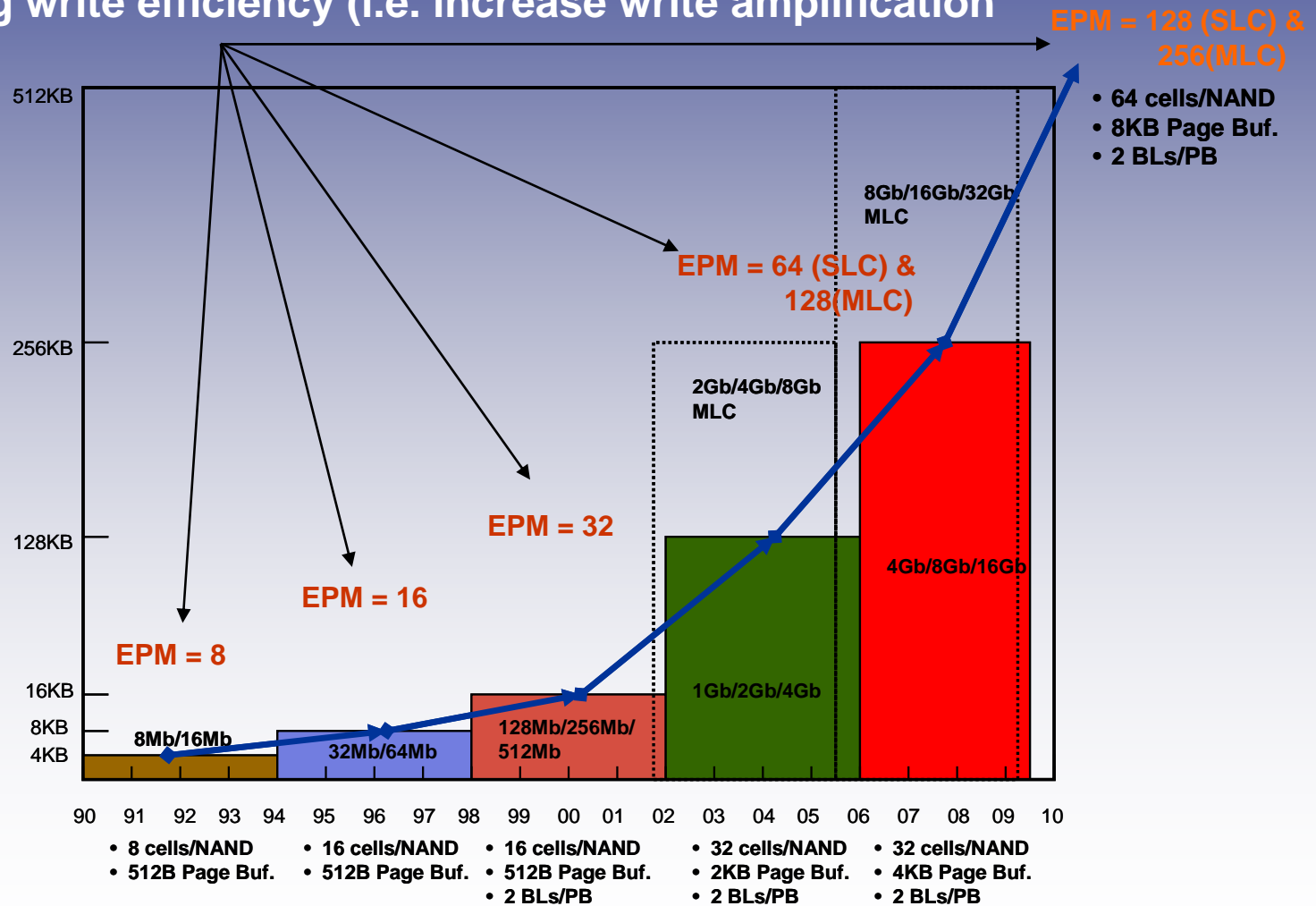


$$\text{Block Size} = (\text{A} * \text{B} * \text{C}) * \text{D}$$

$$\text{Erase Program Mismatch (EPM)} = \text{A} * \text{B} * \text{C}$$

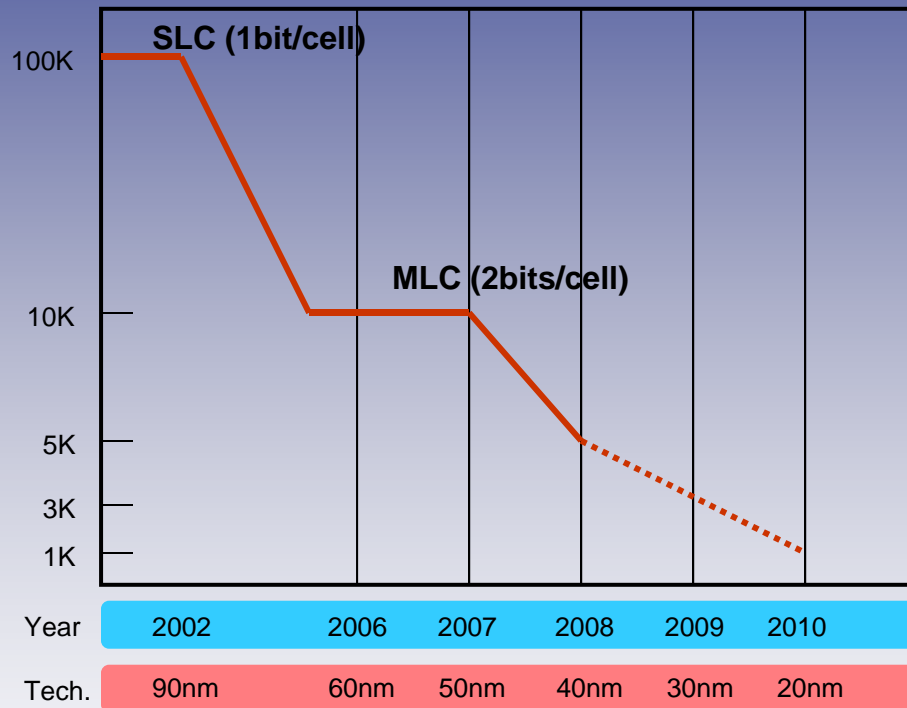
NAND Block Size Trend

Erase Program Mismatch (EPM) is a key parameter to degrading write efficiency (i.e. increase write amplification factor)

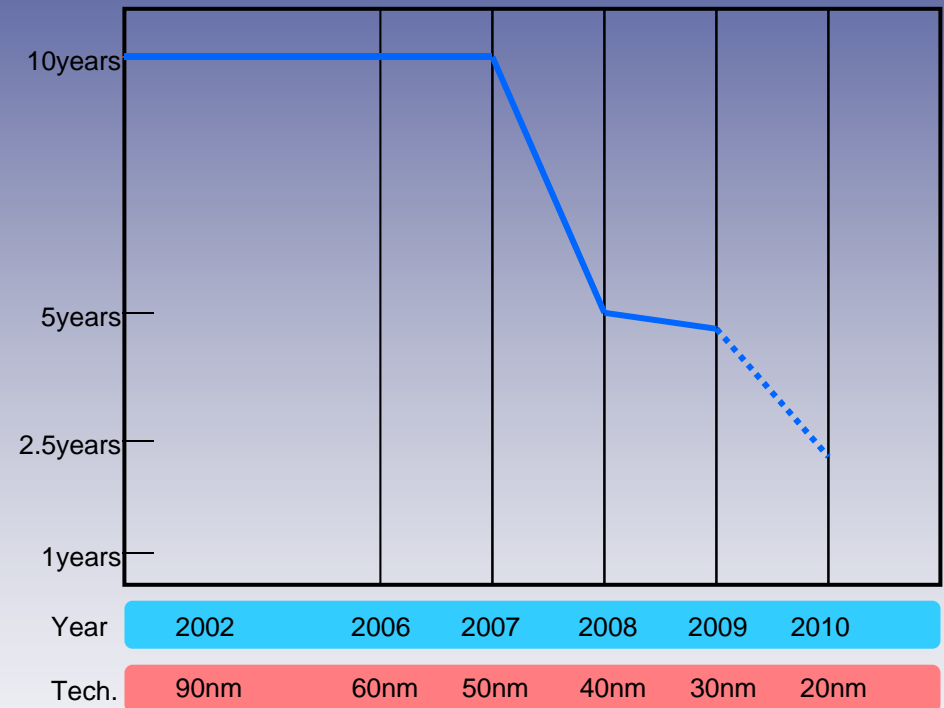


NAND Challenges in Computing Apps

Cell Endurance: # of Reprogram Cycles



Data Retention: Ability to Retain Charge



Reliability degradation combined with the current NAND architecture trend introduces a negative impact on computing applications

Flash System Lifetime Metric

- System lifetime heavily relies on NAND architecture and features

$$\downarrow \text{ Write Efficiency} = \frac{\text{Total Data Written by Host}}{\text{Total Data Written to NAND}} \uparrow$$

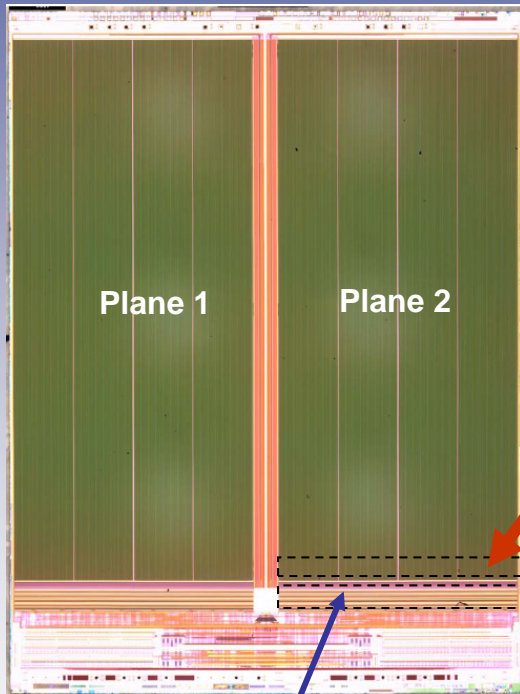
$$\begin{aligned} \downarrow \uparrow \downarrow \downarrow \text{ Total Host Writes} &= \text{NAND Endurance Cycle} \downarrow \\ & * \text{System Capacity} \uparrow \\ & * \text{Write Efficiency} \downarrow \\ & * \text{Wear Leveling Efficiency} \downarrow \end{aligned}$$

$$\text{System Lifetime} = \frac{\text{Total Host Writes}}{\text{Host Writes per Day}}$$

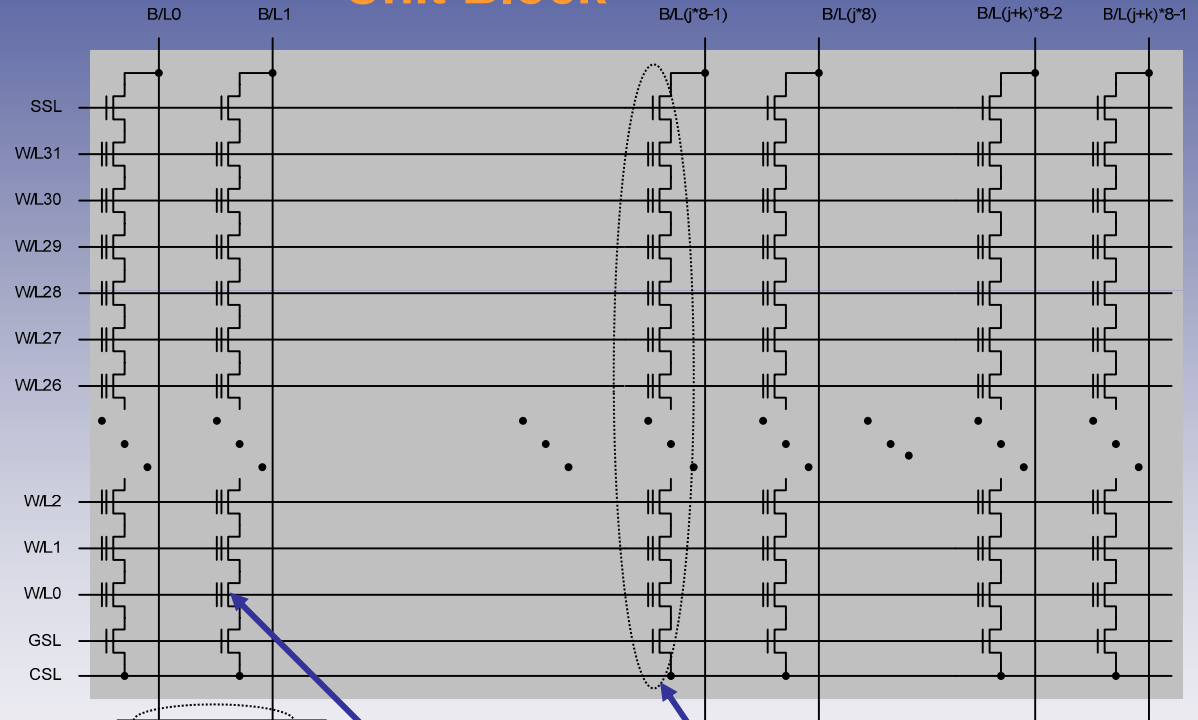
NAND Architecture Innovation

Current NAND Flash Architecture

Unit Block



D: Page (buffer) Size



B: # of Bitline/Page Buffer

A: # of Bit/Cell

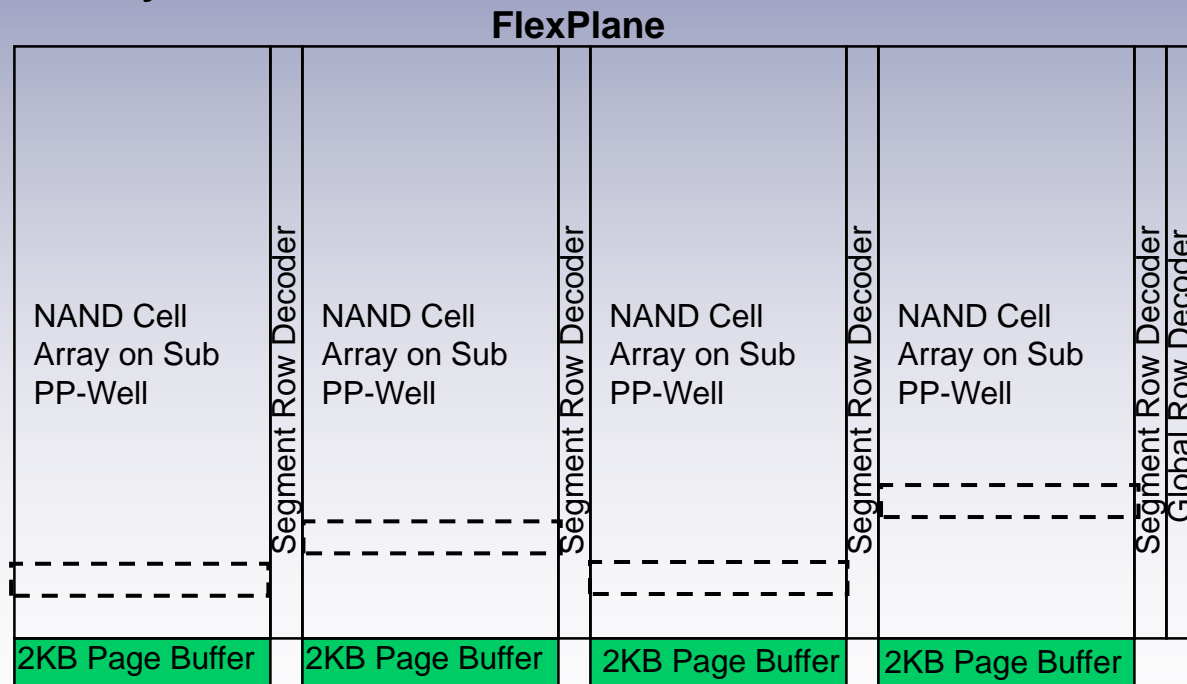
C: # of Cell/NAND String

$$\text{Block Size} = (A * B * C) * D$$

NAND Architecture Innovation

FlexPlane with 2-tier Row Decoder Scheme

- Smaller & Flexible Page Size (2KB/4KB/6KB/8KB)
- Smaller & Flexible Erase Size
- Lower power consumption due to segmented pp-well
- Extend system lifetime



FlexPlane Operations

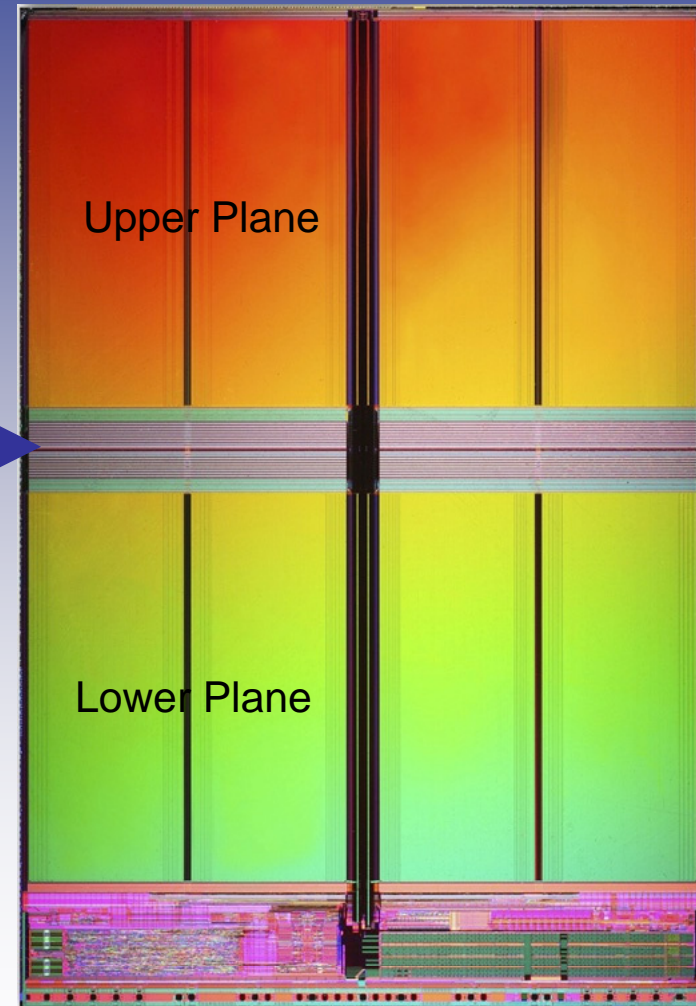
NAND Architecture Innovation

2-Dimensional Page Buffer Scheme

- Higher Performance
- Lower Power Consumption
- Higher Yield

**2-Dimensional Page Buffer
(Shared Page Buffer)**

**0.5x Bitline Length
compared to conventional
NAND architecture**



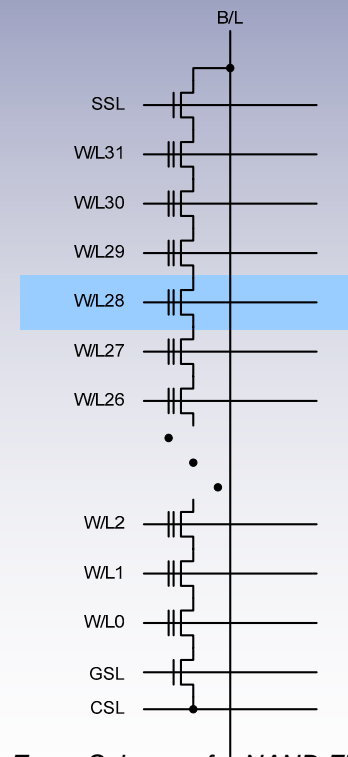
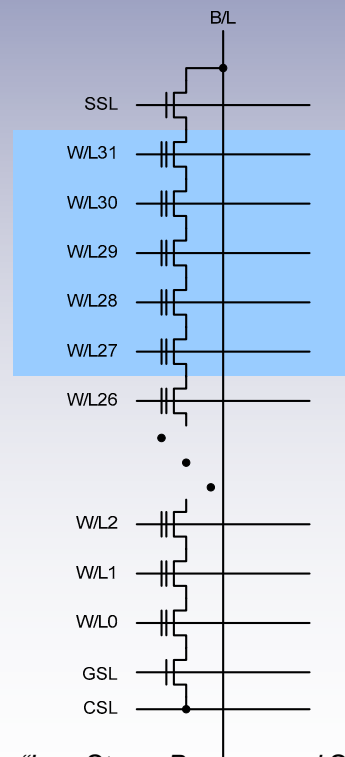
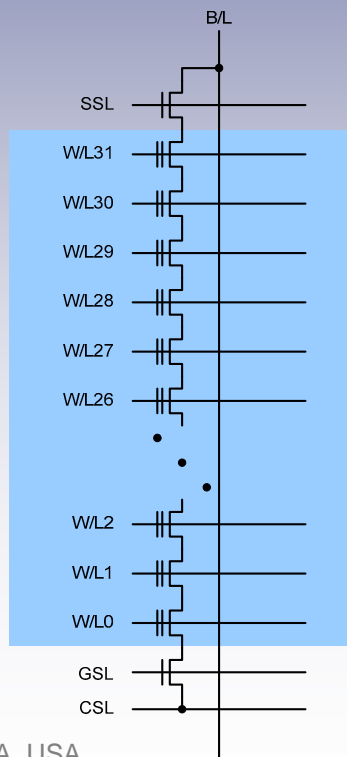
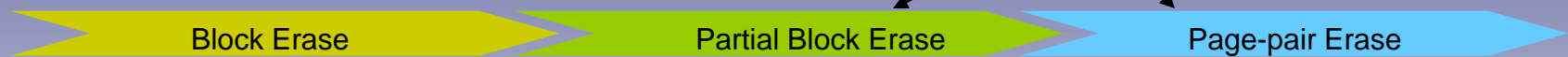
Micron 32Gb NAND Flash in 34nm, 2009 ISSCC

NAND Core Innovation

Page-pair & Partial Block Erase

- Minimize Erase Program Mismatch (EPM)
- Improve write efficiency

• MOSAID's Erase Scheme*

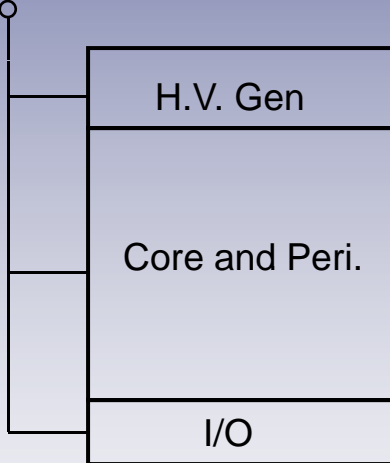


NAND Core Innovation

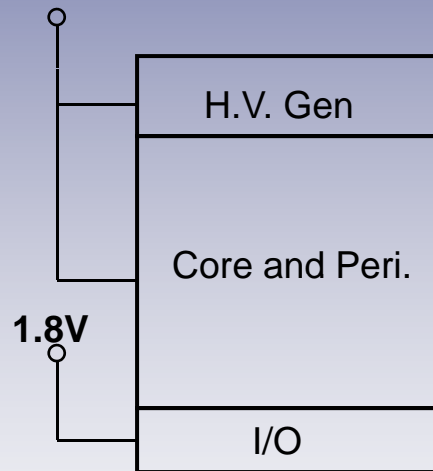
Lower Operating Voltage



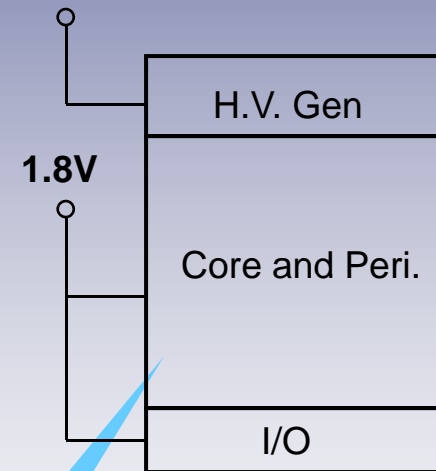
2.7 ~ 3.6V



2.7 ~ 3.6V



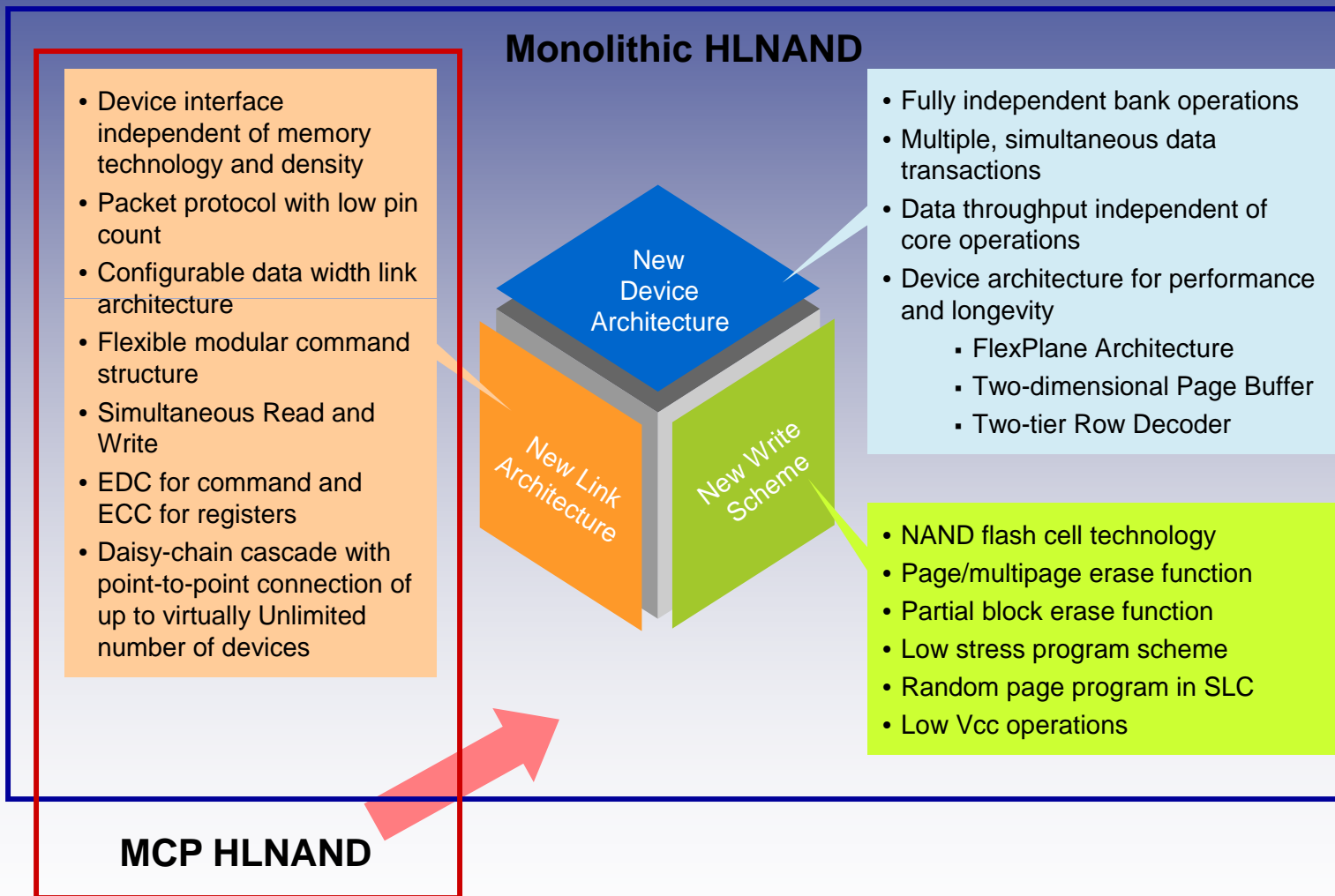
3.3V



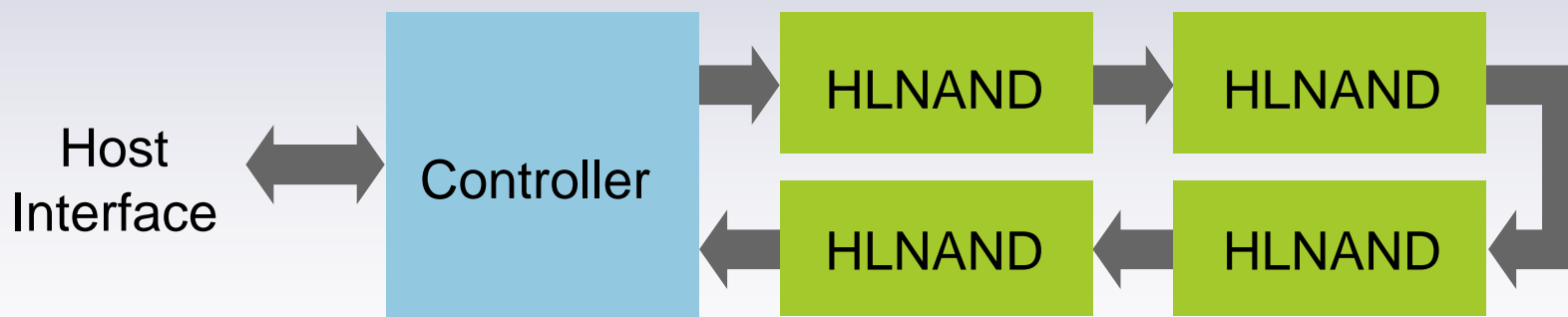
• **MOSAID's Low Stress Program Scheme***

* Jin-Ki Kim, "Low Stress Program and Single Wordline Erase Schemes for NAND Flash Memory", IEEE NVSMW Aug. 2007.

HyperLink (HLNAND™) Flash

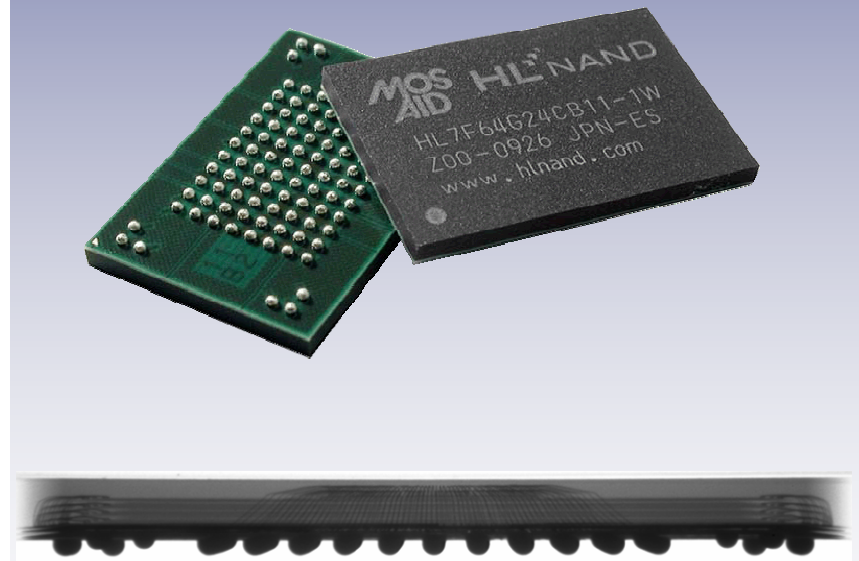
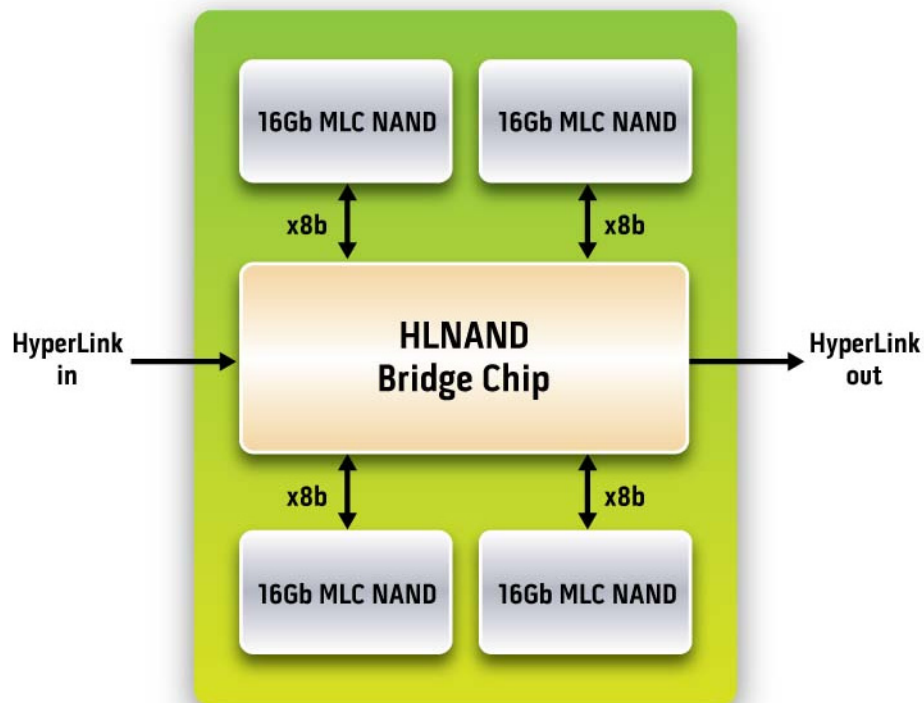


- Point-to-point ring topology
 - Synchronous DDR signaling with source termination only
 - Up to 255 devices in a ring without speed degradation
 - Dynamically configurable bus width from 1-8 bits
 - HL1 parallel clock distribution to 266MB/s
 - HL2 source synchronous clocking to 800MB/s, backward compatible to HL1



64Gb MLC HLNAND MCP

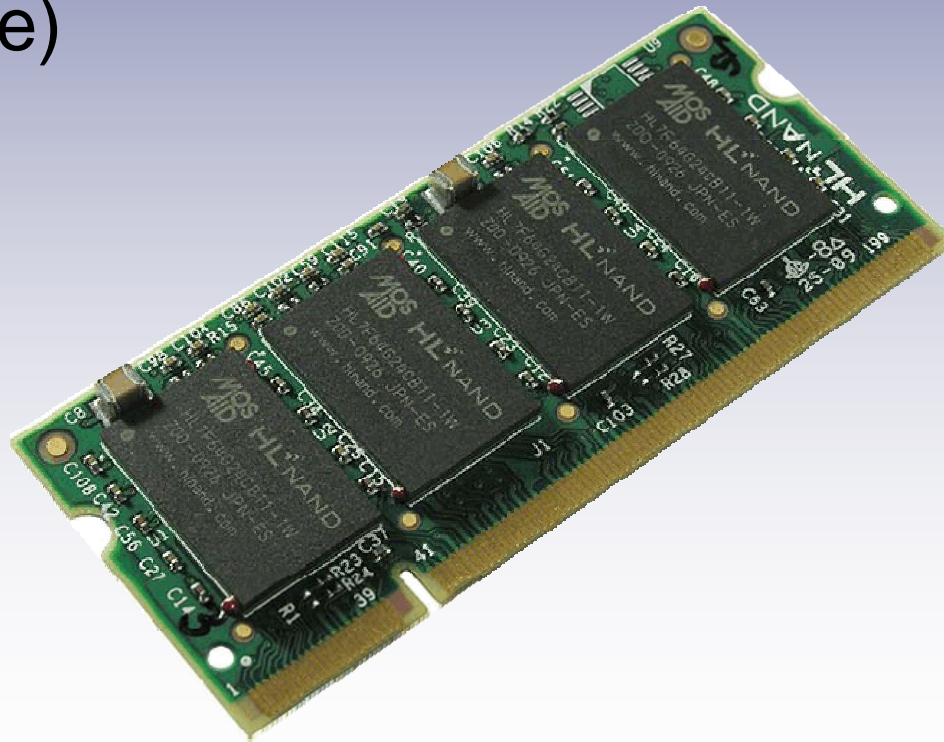
- HLNAND bridge chip MCP with 4-NANDs stacked
- HL1 (DDR-200/266) using NAND in MCP - fully compliant to HLNAND spec



12 x 18 100-Ball BGA

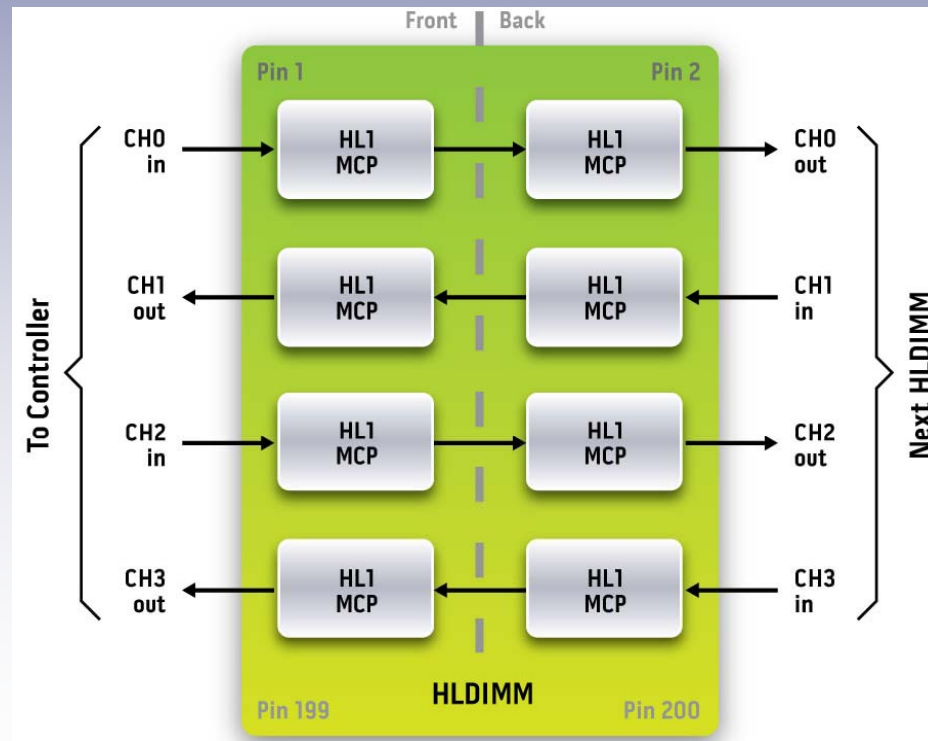
HLNAND Flash Module (HLDIMM)

- Use cost effective DDR2 SDRAM 200-pin SO-DIMM form factor and sockets
- 8 x 64Gb or 8 x 128Gb HLNAND MCP (4 on each side)



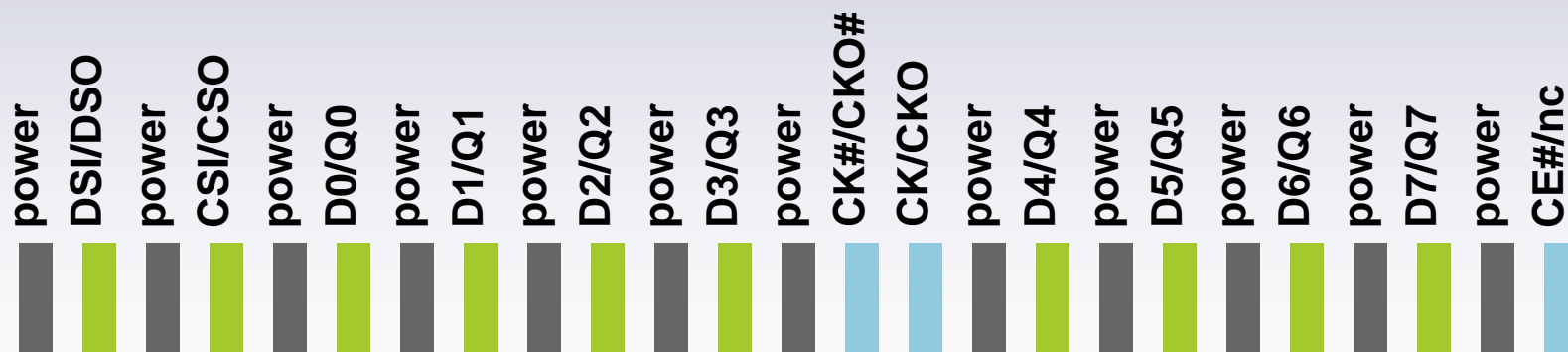
HLDIMM Port Configuration

- Four independent HyperLink interface (266MB/s)
- Aggregate bandwidth of 1066MB/s regardless of # of module



HLDIMM Pin Assignment

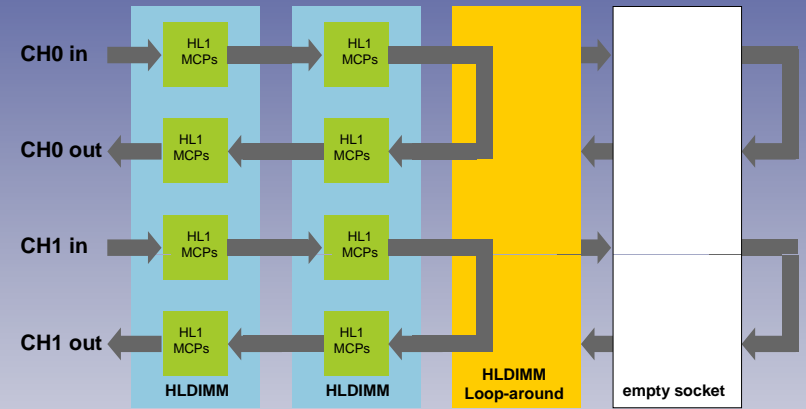
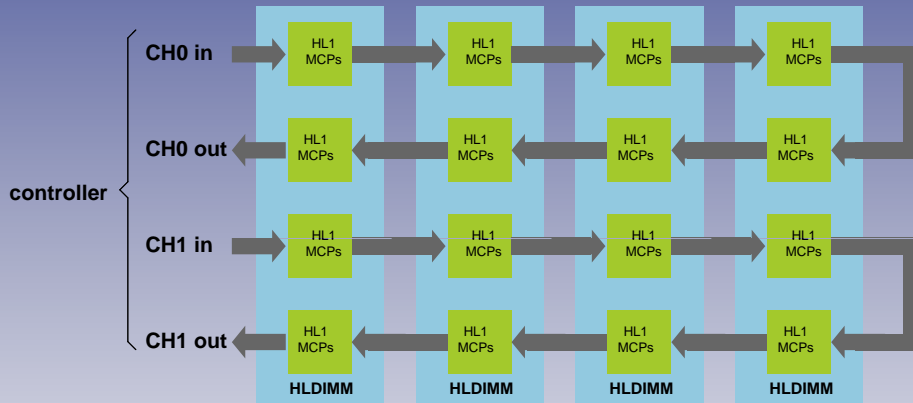
- All high speed signals fully shielded with 1:1 ratio between signal and power/ground
- 6 Vss, 3 Vdd (1.8V), 3 Vdd3 (3.3V) per channel in/out
- Vref and Reset pins shared by all channels
- 5 pin SPD interface
- Forward compatible to HL2 800MB/s source synchronous clocking



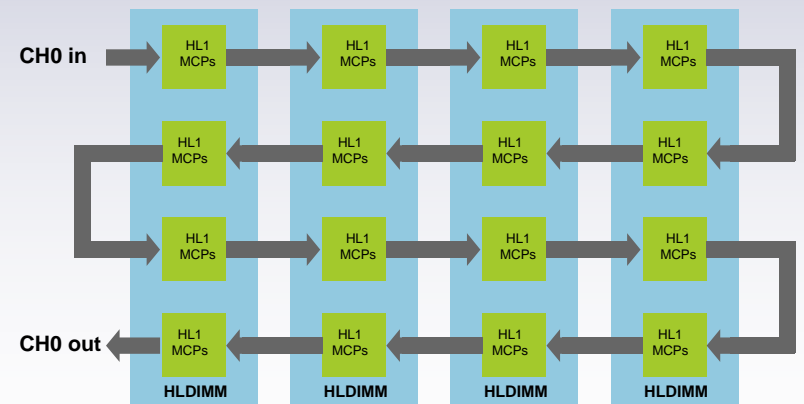
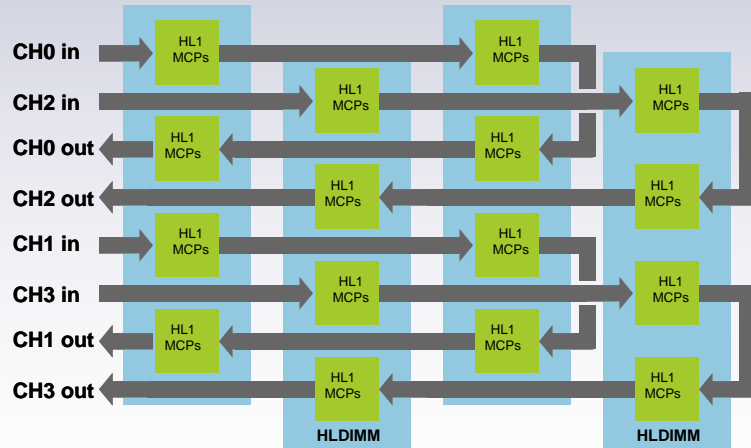
channel input/output pin assignment

System Configurations with HLDIMM

Non-Interleave - 1066MB/s Aggregate Throughput



Interleave - 2133MB/s Aggregate Throughput

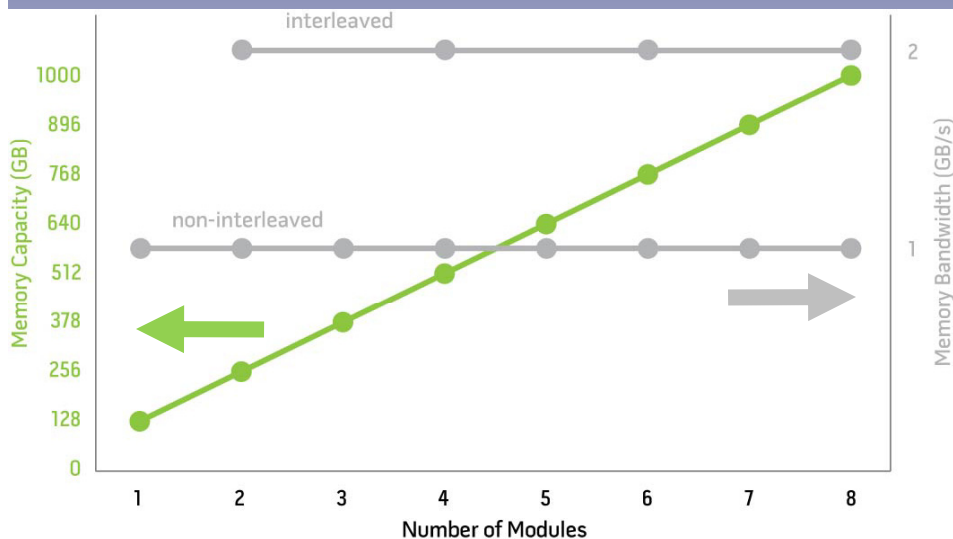




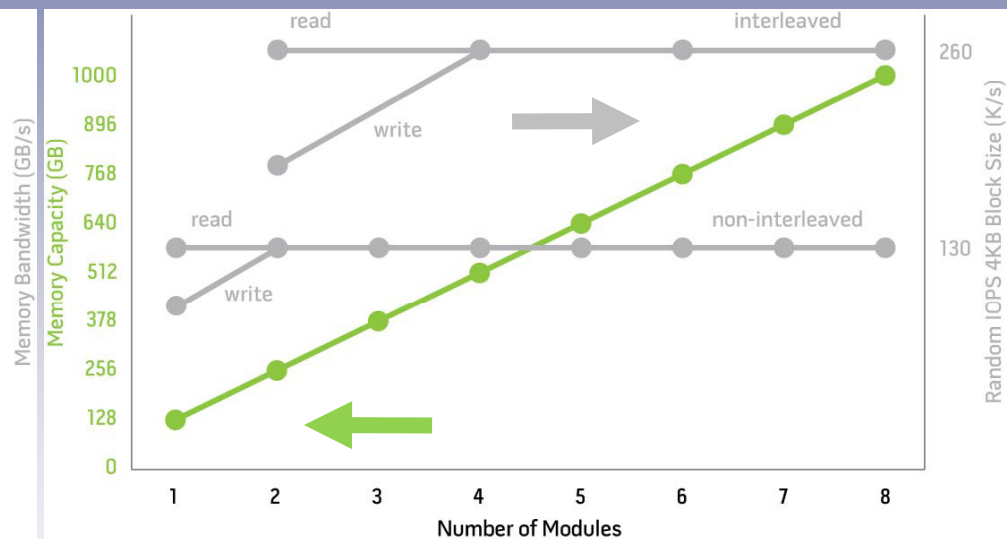
HLDIMM Performance

Capacity, Bandwidth and Random IOPS

Capacity & Bandwidth vs. # of Modules

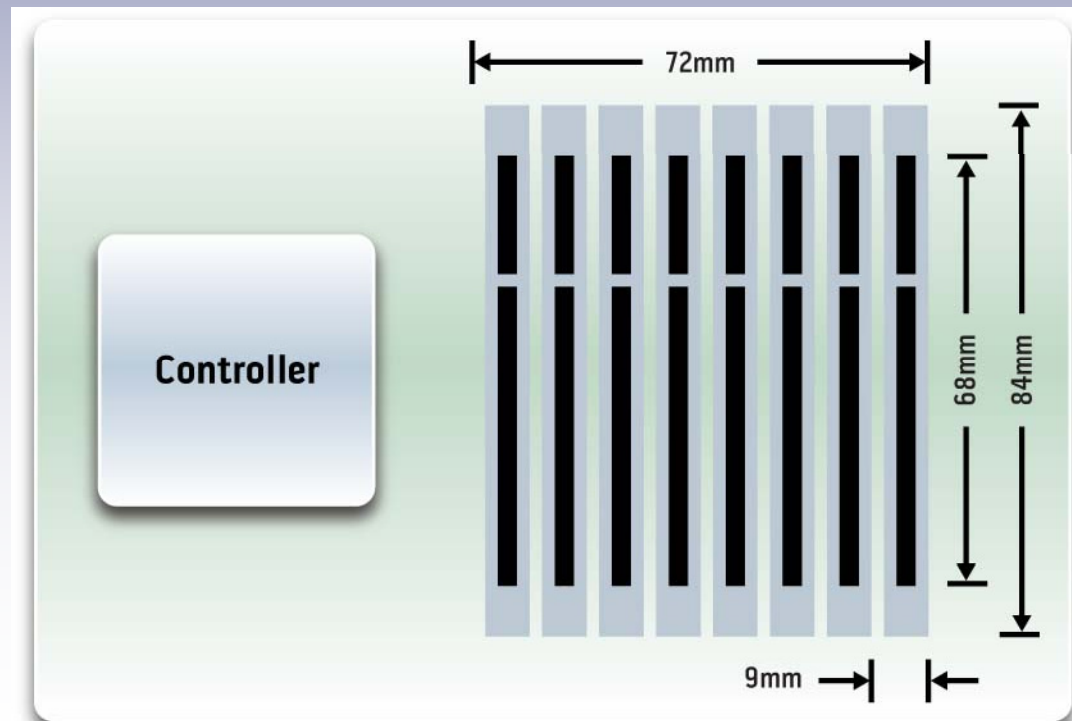


Random IOPS vs. # of Modules



HLDIMM Packing Density

- Fully populated memory capacity of 512GB or 1TB is achieved using 64GB and 128GB HLDIMM modules within only 60cm² of motherboard area.



- The driving forces in future Flash memory are the memory architecture & feature innovation that will support emerging system architectures and applications
- Using HLNAND Flash, Storage Class Memory is viable today using proven NAND flash technology



Resource for HLNAND Flash

www.HLNAND.com

■ Available

- 64Gb MLC MCP sample
- 64GB HLDIMM sample
- Architectural Specification
- Datasheets
- White papers
- Technical papers
- Verilog Behavioral model

