Technology for sub-50nm DRAM and NAND Flash Manufacturing

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Abstract

This paper discusses whether memory technologies can continue advances beyond sub-50nm node especially for DRAM and NAND flash memories. First, the barriers to shrink technology will be addressed for DRAM and NAND flash memories, depending on their inherent operation principles. Then, details of technology solutions will be introduced and its manufacturability will be examined. Beyond 30nm node, It is expected that 3-dimensional transistor scheme is needed for both logic and memory array in addition to the development of new materials and structural technologies.

Introduction

Around 2010, 4Gb DRAM and 16~32Gb NAND flash will be mass-produced with 50nm technology node as shown in Table 1. Recently, much effort has been dedicated to clarify the issues which memory technology for 50nm node and even below will encounter together with suitable solutions. Although there have still been rooms for the successful manufacturing while maintaining cost-effectiveness, most of concerns come from the technical complexity which may not be easy to be avoided in order to meet the ever-demanding product performances, for instance, over 1Gbps of DDR3 DRAM, over 1sec of data retention times of mobile DRAM and over 20MB/s program throughput of 32Gb NAND flash. Furthermore, narrow process window and wide spread-out of process variations to fabricate 50nm memory devices will impose another challenge to successful manufacturing of 50nm DRAM and NAND flash and beyond. Thus, conventional "shrink technology", which is primarily based on dimension scaling, can not solely provide complete answers for sub-50nm DRAM and NAND flash manufacturing. In order for successful manufacturing, "shrink technology" must be supplemented with novel approaches such as new device structures, new process technology and new materials. In this study, technical challenges of 50nm memory technology will be firstly reviewed and details of technology solutions on the new approaches will be discussed in order to fulfill the 50nm DRAM and NAND flash manufacturing.

DRAM

Key design features for DRAM cells are a high storage capacitor and low leakage current at the storage node connected to the capacitor[1,2]. The refresh interval, key parameter describing DRAM performance, is governed by the stored charge loss at the capacitor. The leakage current at the storage node consists of leakage through the capacitor itself, junction leakage current at the storage node, and sub-threshold conduction from a cell transistor. However, as the design rule shrinks down, the capacitance of the storage capacitor decreases due to the reduced effective capacitor surface area and the junction leakage current at the storage node drastically increases due to increased channel doping concentration which is indispensable to block the punch-through of the cell transistor.

The cell capacitor development trend for mass production is shown in Fig. 1[3]. It shows the equivalent oxide thickness, Toxeq, and the dielectric material of the cell capacitor which can fulfill the minimum required cell capacitance of 25fF depending on its technology node. Beyond 100nm, TIT(TiN/Insulator/TiN), one of the MIM structure, capacitor has been utilized and ALD (atomic layer deposition) process has become a mainstream for capacitor dielectric formation due to the nature of relatively high dielectric constant and better step coverage. Beyond 100nm, different kinds of high-k dielectric materials have been developed such as HfO2 and HfO2/Al2O3 around 80nm node, ZrO2 around 60nm node, as shown in Fig. 1. Below 50nm node, RIR(Ru/Insulator/Ru) seems to be one of the promising candidates with Toxeq of 5A at the present time. In practice, the integration complexity of Ru prevents its implementation into a mass production.

Until now, we have successfully achieved the required capacitance of 25fF and even more due to dedicated effort for high aspect ratio OCS capacitor process as well as for development of manufacturable high-k dielectric materials. As device scaling, we have encountered a new hurdle to increase the height of the cell capacitor due to mechanical instability of storage node with high aspect ratio. Since the effective capacitance primarily depends on the height of the cell capacitor as shown in Fig. 2, it is unavoidable to face storage capacitance limit. In order to overcome this physical limit, high-k dielectric material with low leakage is indispensable for future scaling. Instead, novel structure called MESH-CAP is expected to extend existing TIT structure to 50nm node. This novel structure terminates the persistent problems caused by mechanical instability of storage node with high aspect ratio since MESH-CAP is inherently lean-free. The feasibility of this structure was verified using 80nm DRAM technology as shown in Fig. 3[4].

From the leakage current point of view, doping profile at the storage node is the main cause and is determined by the channel doping concentration of a cell transistor and out-diffusion from the poly-silicon plug contact. As shown in Fig.4, a planar transistor can not satisfy the leakage current requirement below 100nm since maximum electric field abruptly increases. Adopting intelligent transistor design such as asymmetric channel and source/drain doping engineering made it possible to use planar transistor around 90nm. Then, new 3-D cell structures called RCAT, S-RCAT have been introduced as shown in Fig. 5[5,6]. RCAT scheme lengthens the effective gate length of the cell transistor and solves the short channel effect without area penalty. The proposed RCAT and modified S-RCAT have been successfully implemented in 80nm 512M and 70nm 2Gb DRAM and seem to make it possible to scale down to 50nm. Beyond 50nm node, FinFETs will become another alternative for a cell transistor. FinFETs, double-gate UTB, are considered as promising solutions for sub 50nm regime in CMOS scaling because of good immunity of short channel effect resulted from the excellent gate controllability with thin body silicon[7]. The feasibility for FinFETs as a DRAM cell transistor was verified using 60nm node, recently as shown in Fig. 6[8]. It has a superior current driving capability as well as short channel immunity over those of RCAT as shown in Fig. 7.

Another leakage source aforementioned was out-diffusion from the poly-silicon plug contact at the storage node. Elevated source/drain structure using selective epitaxial growth is considered to be a possible answer. Using this structure, the short channel effect can be effectively suppressed by forming shallow junction, and it gives a room for transistor engineering for extremely low-doped channel like FinFET. In addition, more wide process window for memory cell contact stability will be guaranteed. The fabricated

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DRAM cell structure is shown in Fig. 8.

NAND Flash

For NAND Flash memory, the physical scaling challenges, the electrical scaling challenges, and the reliability scaling challenges should be addressed[9,10]. Firstly, the physical scaling challenges are considered. As word line space scales down, the capacitance coupling among unrelated floating gates is increased, which causes to shift cell threshold voltage (V_{th}) and widen its distribution. What should be done to reduce this coupling is to decrease the height of the floating gate and adopting low-k dielectric materials. Fig. 9 shows the required height of floating gate to suppress unwanted V_{th} shift below 0.2V induced by the coupling. For 30nm node and beyond, floating gate height will be eventually limited. From the aspect of materials, another possible alternative is to use low-k dielectric materials, which help lessen coupling ratio as shown in Fig. 10. Silicon oxide spacer showed reduced floating gate coupling ratio compared with silicon nitride spacer. Furthermore, structural innovations like SONOS-type cell structure where floating gate is replaced with silicon nitride and charges are stored in the trap sites of SiN can inherently eliminate floating gate interference possibility.

Another physical challenge is that the sidewalls of floating gate along the word line direction cannot be correctly fabricated because the physical thickness of inter-poly dielectrics will be larger than the space between floating gates. Since the contribution of sidewall to coupling ratio from control gate to floating gate is reduced by lowering floating gate height, the coupling ratio will be drastically dropped to below 0.3 at 30 nm node as shown in Fig. 11. To enhance the coupling ratio, inter-poly ONO dielectrics needs to be scaled down to 15nm. But ONO thickness was limited by 13nm physically. As another approach, high-k dielectric materials like Al2O3 and HfO2 can be adopted. Recently, new cell structure called U-shaped NAND flash with increased coupling ratio through inter-poly dielectric area enhancement has been proposed and tested as shown in Fig. 12. The result confirms the process feasibility of by using sub-55nm 16Gb NAND flash.

Regarding electrical scaling challenges, as cell dimensions are scaled down, short channel effect due to short gate length and driving current reduction due to narrow active width become serious. Below 30nm node, those challenges will be grave enough to degrade the sensing margin and the device operation speed. In the multi-level cell operation, it becomes even worse. To overcome short channel effect and driving current reduction, booster plate structure and FinFET-type flash seem to be promising[11,12]. Since FinFET structure uses the sidewall channel as well as top planar surface, the driving current can be increased and eventually becomes irrespective of device scaling. In addition, its superb controllability of thin silicon body gives strong immunity to short channel effect. In booster plate structure, the short channel effect was reduced due to suppressed programming interference in unselected cells. Fig. 13 shows the proposed booster plate structure and FinFET-type NAND flash cell structure, for example.

From the standpoint of the reliability scaling, the challenge is posed by significant decrease of number of electrons on the floating gate because of decrease of the inter-poly ONO capacitance as shown in Fig. 14. It is expected that less than 100 electrons for V_{th} shift of 6V will be stored at 30 nm design rule. Since a charge loss tolerance becomes less than 10 electrons, data retention and endurance failures are prone to happen. A possible way to suppress charge loss via tunnel oxide, intensive interface engineering between tunnel oxide and silicon surface has been suggested.

As far as peripheral device scaling is concerned, besides aforementioned scaling challenges related to cell itself, high electric fields required for programming and erasing cause scaling in peripheral device to lag behind in order to support high voltage requirement. Meanwhile, tunnel oxide could not be scaled aggressively due to data retention constraints. New cell structure like SONOS and high-k dielectric material development will give a room for scaling the high voltage peripheral devices.

In summary, for NAND flash, conventional floating gate will be continuously scaled down to 50 nm node. Beyond that, it is projected that SONOS-like NAND Flash will be overwhelming. Fin-type cell structure will be supplemented to the SONOS-like cell and help it extend scaling below 20nm node. The manufacturability for 4Gb SONOS-like cell has been successfully demonstrated by using 60nm design rule[13]. Fig. 15 shows the new approach called TANOS cell where a dielectric composite of SiO2/SiN/Al2O3 and TaN electrode was adopted, its high-k dielectrics with good band gap matching between blocking oxide and charge trapping layer improves the coupling ratio onto the tunnel oxide. As a result, the dielectrics are allowed to be thicker for improving charge loss and getting faster erase. This is a positive sign for the future NAND development that the well-known weak points of SONOS cell will be overcome near future.

Conclusions

Technical challenges for sub-50nm node have been substantially reviewed and novel approaches to overcome those scaling barriers such as new device structures, new process technology and new materials have been suggested and fully examined. DRAM and NAND flash memory are expected to maintain their dominant position in portable mass-storage markets beyond sub-50nm node. However, beyond 30nm node, there seems to be a long way to solve ballooning wafer process difficulties posed by the pressure for ever-decreasing feature size and the demand for new materials. Novel solutions to break these barriers have been suggested and started to show their promises. Those will allow both DRAM and NAND flash to extend scaling and provide cost-effective data-storage solutions.

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Table 1. Technology roadmap for future DRAM and NAND flash memories.

	Year	04	06	08	10	12
	Node (nm)	80	65	50	40	30
	Lithography	ArF	ArF Immersion	F2 Immersion , EUV		
	Gate	Wsix+Si	W+Si	W+WN / CoSix		
	Metal / IMD	Al			Al or Cu / Low-K	
DRAM	Density	1Gb	2Gb / 4Gb	4Gb / 8Gb	16Gb ~	
	Cell Structure	RCAT		FinFET		
	Capacitor	MIS	MIM (AHO / HfO / TiO2)			
NAND	Density	2Gb	4Gb / 8Gb	16Gb	32Gb ~	
	STI	Self-Align	Advanced Self Align			
	Cell Structure	Floating Gate			SONOS + FinFET	
	Tunnel Oxide	8nm	7nm Radical Ox. + NO		3nm Radical Ox.	
	Inter Dielectric	O/N/O		Thin ONO or High-K	-	

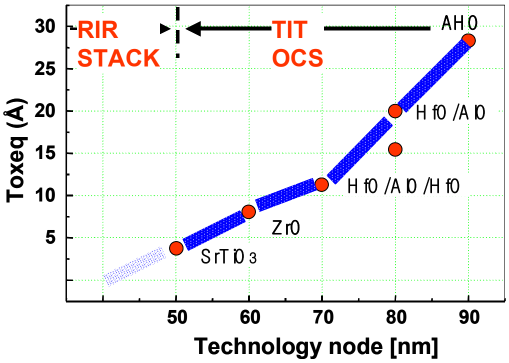


Fig. 1. DRAM cell capacitor development trend describing the equivalent dielectric thickness and the height of a cell capacitor.

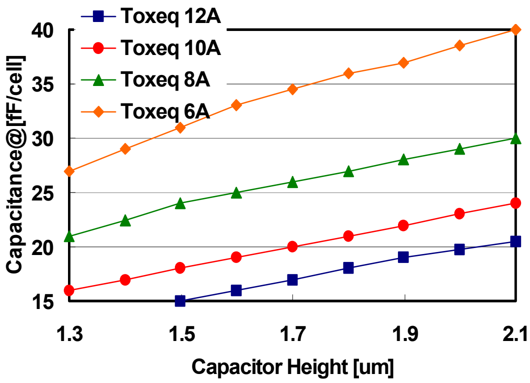
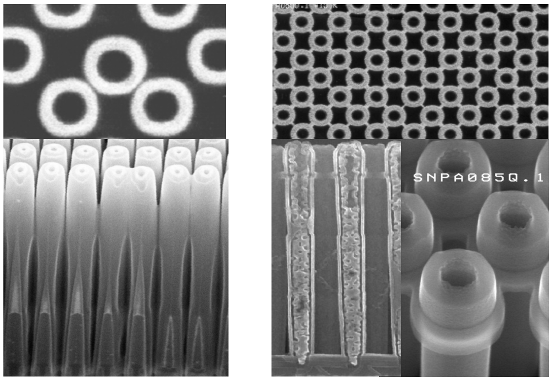
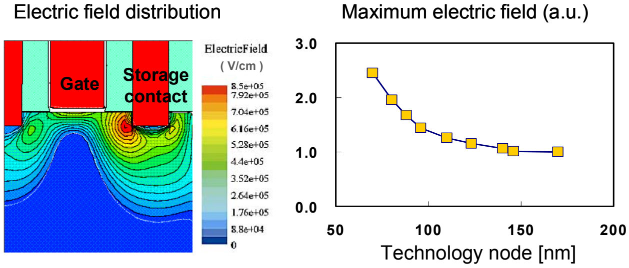


Fig. 2. Relationship between the cell capacitance and the height of the cylindrical capacitor at 50nm design rule.



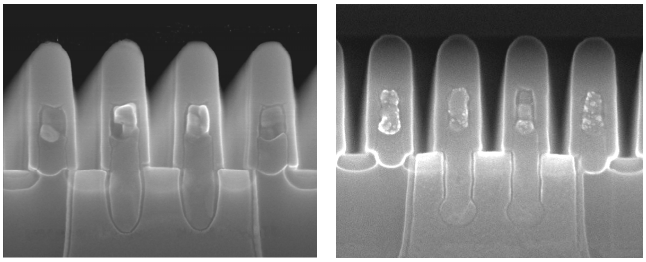
(a) (b)

Fig. 3. (a) Top and vertical SEM view for conventional OCS capacitor, (b) top, vertical, and tilted SEM view for MESH-CAP fabricated at 80nm design rule.



(a) (b)

Fig. 4. (a) Electric field distribution in DRAM cell transistor, (b) maximum electric field at the storage node as a function of technology node, normalized to 150nm node.



(a) (b)

Fig. 5. (a) Vertical SEM view for the fabricated RCAT DRAM cell, (b) vertical SEM view for the fabricated S-RCAT DRAM cell, respectively.

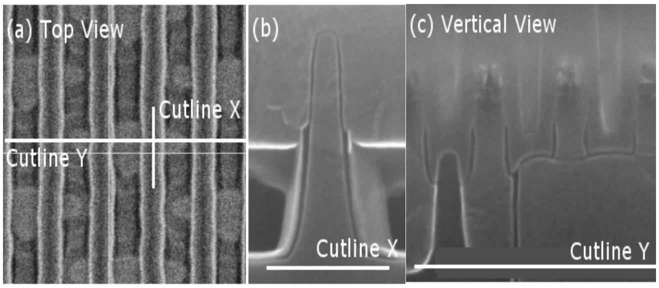
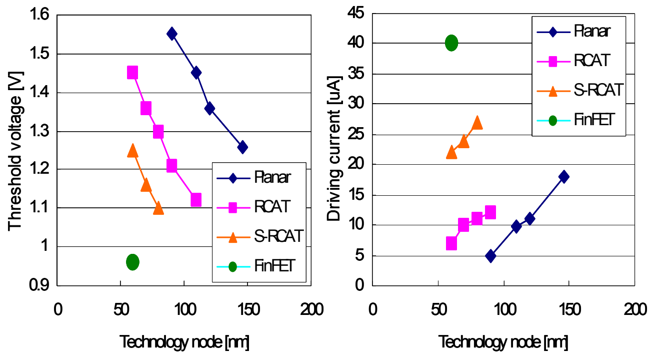
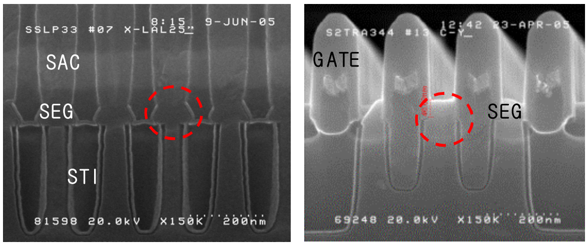


Fig. 6 Fabricated D-FinFET structures using sub-60nm design rule. (a) top view shows the damascene and gate patterns. (b) vertical view showing the active fin-structure along the gate line, (c) vertical view perpendicular to the gate lines.



(a) (b)

Fig. 7. (a) Threshold voltages, (b) driving currents for various DRAM cell transistors depending on technology node are shown. The driving current was measured at 1.2V.



(a) (b)

Fig. 8. (a) Vertical SEM view of the bit-line contact for the DRAM cell, (b) vertical SEM view of DRAM cell transistors with an elevated source/drain structure using selective epitaxial growth.

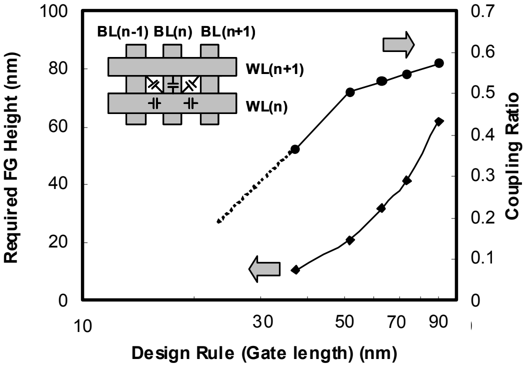


Fig. 9 Required floating-gate height for the effective suppression floating gate-poly coupling interferences and coupling ratio by design rule.

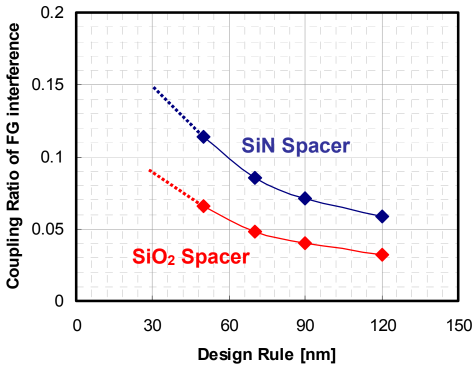
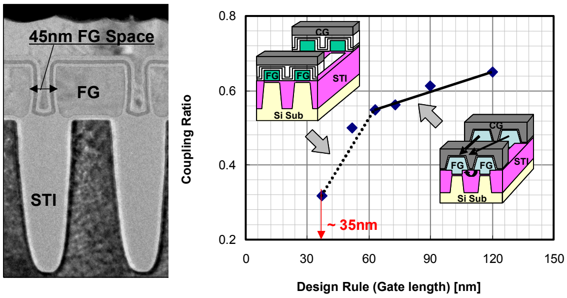
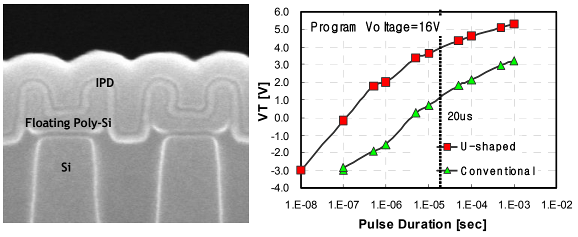


Fig. 10. Reduced Floating gate interference due to low-k dielectric material.



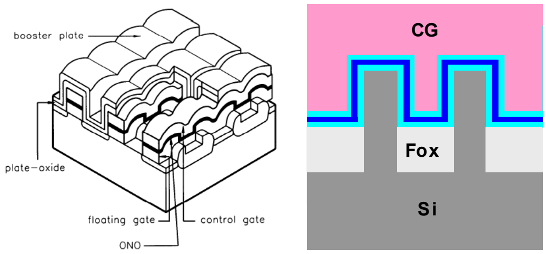
(a) (b)

Fig. 11 (a) Vertical SEM view for the NAND flash cell in WL direction, (b) inter-poly coupling ratio as a function of design rule.



(a) (b)

Fig. 12. (a) SEM image of U-shaped floating gate poly-Si structure, (b) programming curves of U-shaped floating gate poly-Si structure NAND flash device, fabricated using sub-55nm design-rule.



(a) (b)

Fig. 13 (a) Schematic view for the booster plate implementation, (b) vertical schematic view for new NAND flash memory with Fin-type structure.

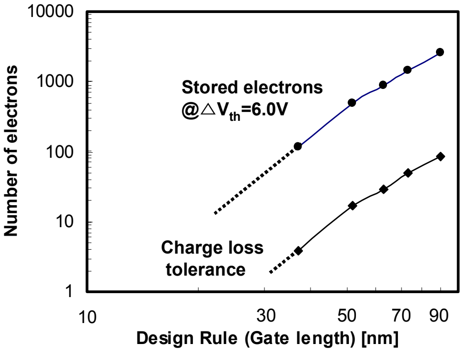


Fig. 14. Number of stored electrons in a NAND flash cell and the amount tolerable for charge loss by technology node.

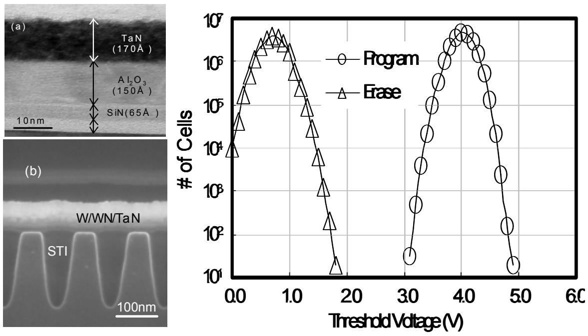


Fig. 15 (a) Cross-sectional TEM image of TANOS cell profile, (b)SEM image of TANOS STI profile, (c)distribution of threshold voltage in 2Mb cell array after programming and erasing pulse, where TANOS cell was fabricated using 63nm design rule.