Post-etch residue and photoresist removal challenges for the 45 nm technology node and beyond

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ABSTRACT
Removal of photoresist (PR) and residues is becoming very critical in future generations of devices. In front-end-of-line (FEOL) post ion implantation (source/drain, extensions, halos, deep wells), the use of PR to block off parts of the circuit results in PR which is substantially hardened and difficult to remove. In back-end-of-line (BEOL) etching, the selectivity to removing resist and residues without removing low-k materials is very challenging. An overview of the status, issues and some novel approaches are presented.

Introduction
Photoresist is used to protect some areas of the wafer from dry etch chemistries, ion implants, etc. After completion of the process, the photoresist needs to be selectively removed and the surface cleaned, ensuring a residue and particle free surface. Removal of resist is in principle possible using wet chemicals such as hot SPM, organic solvents or by ‘ashing’ using dry plasmas. However, resists are chemically modified during dry etch or implant processing, and such modification can dramatically reduce strip rates. If more aggressive — e.g. highly oxidizing — chemistries are used instead, this may lead to undesirable attack of other materials on the wafer. While such considerations have been important for unit process development for several decades, certain ITRS roadmap requirements for the 45nm technology node and beyond are becoming so stringent that a fundamental paradigm shift in several modules of the CMOS integration flow is under consideration in industry labs. At the same time, new alternative integration schemes, including the use of strained silicon, metal hardmasks and metal gate electrodes, result in different requirements. This further complicates the study of this topic.

In the following, we summarize the status, issues, and novel approaches, focusing on the source-drain implant module in FEOL and on the low-k dry etch module in BEOL.

FEOL: Post-implant resist strip
The source-drain (S/D) junctions of FETs are created by ion implantation of dopants into the Si substrate. Such implants typically involve ions such as As, P, B, or BF₂ with areal densities of ca. 10¹² to several 10¹⁵ cm⁻². Ion energies range from a few 100eV for very shallow S/D extensions to several tens of keV for deep implants. To ensure that the various devices being fabricated on the same chip/wafer, in particular nFETs and pFETs, each receive only the appropriate implants, selective implantation is required. This is achieved by masking with patterned photoresist, as schematically illustrated in Figure 1.

The complex dopant geometries in the S/D regions are therefore created by cycles of photoresist application and patterning, ion implant, resist strip and surface cleaning.

The ions implanted in the resist result in chemical modification in the near-surface regions. Chemical bonds of the resist polymer are broken by the energy from the impinging ion, which can lead to polymer main chain scission.

Figure 1. Schematic showing a selective junction implant into nFET while the pFET is protected by photo resist (not to scale).
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side group detachment, cross-linking, etc. Outgassing therefore occurs during implant. Most prominently, the hydrogen content of the resist drops sharply for high areal density/high energy implants, e.g. for 10–100 keV As implants in the \(10^{15}–10^{16} \text{cm}^{-2}\) range [1, 2]. These chemical modifications entail structural changes; the resist layer is thinned and its edges may blur (Figure 2) [3]. Most importantly, a heavily modified, hardened layer with low H content, often referred to as a ‘carbonized crust’, is formed in the upper resist region and at exposed sidewalls [1, 2]. The H loss from this layer, whose thickness is largely determined by the ion range in the resist, can, for example, be measured by time-of-flight secondary ion mass spectrometry (TOF-SIMS). Though oxygen atoms and other species remain in the layer, the high C content results in the formation of nano- or microcrystalline graphite-like material (i.e. containing extended units with predominantly \(\text{sp}^2\)-hybridized C-C bonds), which we have detected by Raman spectroscopy (Figure 3) [3].

Importantly, typical wet photore sist strip chemistries fail in the presence of such crusts (Figure 4). For example, strip rates in hot Piranha solutions \((\text{H}_2\text{SO}_4, \text{H}_2\text{O}_2)\) or in organic solvents nearly vanish for high implant doses. In addition, implant ions remain in the resist where they can form compounds that are not easily removed by wet-chemical means, leading to detrimental residues [4].

Removing silicon next to the gate (i.e. underneath the spacer), commonly referred to as the silicon recess, is believed to result in a drop of device current as a result of a geometric effect. This implies that the PR removal after the gate etching and after extension and halo implantations should have very high selectivity with respect to spacer oxide and STI oxide is required as well.

**Current approach**

To achieve sufficient crust strip efficiency, and hence acceptably low cycle times, as well as good residue removal, aggressive plasma strip chemistries are being employed in combination with wafer heating. These typically involve plasmas based on highly oxidizing O radicals [1]. To enhance the crust strip, F-containing species are added to the plasma. However, these tend to attack the exposed oxidized Si substrate. To alleviate the issue, a two-step process with an F-containing crust strip followed by an F-free bulk strip is commonly employed [5]. However, substrate etch is not entirely prevented. Moreover, since the oxidation of silicon should also be regarded as Si substrate loss, the oxidation should be limited too.

**New trends for 45nm node and beyond: Issues and opportunities**

With further down-scaling, implants are becoming shallower and consequently silicon loss results also in loss of dopant [6]. The S/D doses are expected to be maintained with a maximum level of about \(5 \times 10^{15} \text{at/cm}^2\). The increased doping level at the surface typically results in higher Si etch rates [7]. As a result, it is becoming progressively harder to meet Si loss targets in the source-drain module with conventional stripping methods.

The limits on Si substrate loss in the S/D implant module are particularly stringent after the shallow extension implants. For example, the ITRS specifies a Si loss per clean in 2006 of less than 0.7 Å and in 2010 of less than 0.3 Å. Since Si oxidized by the plasma is readily etched by F radicals or during the final wet clean, it is becoming progressively harder to meet Si loss targets. The expected advent of advanced gate stacks that incorporate metal gates poses an additional challenge, since they are often very sensitive to oxidation and corrosion [8]. An additional concern, recently reported, is the significant B-loss during the PR wet cleaning process, in the absence of a chemical oxide [9].

For the 45nm node it is very likely that in-situ doped SiGe epi grown junctions will be used for the p-MOS transistor to generate the desired strain. Although SiGe in itself is more vulnerable to attack than Si, this integration scheme would eliminate S/D implantation. Whether a reciprocal
approach can be applied to the n-MOS transistor to generate opposite strain remains to be seen. At the same time the implantation energies are reduced (e.g. plasma-doped (PLAD) implant) as junctions become shallower and this may create new opportunities as the hardening of the resist is reduced with decreasing implantation energy.

All of these changes require the investigation of new approaches for PR removal. In summary, one could anticipate that more ‘gentle’ removal processes should be explored to obtain an acceptable solution.

BEOL: Post-dry-etch resist and residue strip

Current state of the art

When removing PR and etch residues after low-k dielectric etching, several challenges need to be addressed. First, good removal of the PR and etch residue needs to be obtained while maintaining good CD control. This implies that not too much (damaged) low-k dielectric material should be removed during the residue removal step, which in turn implies that the damage should be kept to a minimum. The k-value of the material should be preserved, which typically means no liquid or liquid residues should remain in the low-k material, and damage should be minimized and preferably be repairable. Finally, another critical issue is the fabrication of a good pore sealing before barrier deposition. This is needed for a good metal barrier deposition and to prevent metal from being built into the low-k ridges and avoid shorts.

Two approaches to seal and implement the strip process can be considered [5] (Figure 5). In the first approach, the pore sealing is done after the removal of PR and residue. In this case one can expect liquid to penetrate into the low-k material, potentially resulting in more damage. Therefore, restoration of the k-value needs to be performed, which implies removal of the remaining liquid and residues and possibly also chemical repair of the low-k material. In the past, successful repair of porous MSQ materials with fairly large pore size has been demonstrated [10, 11]. The trend is towards smaller pore size (1–2nm). For such materials, no good repair process has been found, up to now [12]. In a second approach, the pore sealing is obtained during the dry etch process prior to the removal of the PR and residue. In this process the residues need to be removed selectively to the sealing layer. In this way, possible degradation of the low-k dielectric by the chemicals is prevented.

Overall ‘selectivity issues’ are very severe. Indeed, low-k films contain significant amounts of carbon and/or methyl groups. This makes them resemble the chemical nature of the photoresist and post etch residues that need to be removed. Using conventional ashing processes containing O2 source gas effectively removes the residues but also leads to severe oxidation of the low-k material, which can be seen with different analytical techniques (FTIR, XPS, EFTEM,...) (Figures 6 and 7). This results in a decrease of CH2-groups, an increase in O and often an increase in OH, leading to an undesirable increase in k-value. Also, the material becomes more hydrophilic and wet cleaning chemicals tend to penetrate into the pores. The ashing degrades the chemical stability of the films making them much more vulnerable to attack during subsequent wet chemical cleaning (loss of CD control). It is desirable to preserve the high contact angle of the low-k material. A reduction in contact angle is believed to result in a stronger tendency for moisture absorption from the air and from subsequent wet treatments such as cleaning and CMP, which potentially can lead to degraded leakage and reliability performance.

More recently, ‘reducing’ ashing – based on H2 – has been introduced as an alternative [13]. This type of ashing indeed seems to better preserve the

![Figure 4. Optical micrograph of patterned and As-implanted (40 keV, 10¹⁶ cm⁻²) KrF resist (orange) on poly-Si lines (brown) after extended treatment with hot SPM: Partial resist removal and crust roll-up.](image)

![Figure 5. Two approaches to implement sealing and strip. In a first approach the pore sealing is done after the removal of PR and residue. In a second approach the pore sealing is obtained during the dry etch process.](image)
chemical nature, and thus the low-k film's properties.
In some cases the dry strip is performed in the etch chamber. Since
the two processes, etch and ash, have different requirements, e.g. in terms
of anisotropy and selectivity, this can lead to somewhat less optimal
stripping conditions, such as reduced wafer temperature and higher bias to
compensate for the loss in strip rate as a result of the reduced temperature,
with possible reduced selectivity as a consequence.

Potential alternative solutions and their issues
Several new approaches have been proposed and are under investigation.
In general, approaches avoiding or minimizing exposure to plasmas seem
to be favoured.

1. For FEOL applications, enhanced wet oxidation strip chemistries such
as ‘enhanced hot SPM’ (i.e. higher temperature, higher concentration
of active species) has been shown to provide superior stripping capabilities
[14–16]. Obviously, compatibility with the use of metal gates is of major
concern and needs to be investigated.

2. Another approach for FEOL applications is the combination of wet
strip and physical force, such as CO₂ snow cleaning followed by hot SPM
cleaning [17]. The process conditions need to be tuned to avoid damage to
fragile structures, such as narrow gate electrode lines. In this respect, one
should keep in mind that, according to the roadmap, at the 65nm node the
gates are printed at 42nm and when trimmed and etched have a physical
width of only 25nm: this is expected to shrink at the 45nm node to 30nm
printed and 18nm physical dimension.

3. Another new approach, applicable to FEOL and BEOL, is based on a
modified forming gas based stripping that converts the residues into
cluster-like particles. These particle-like residues are then removed with a
CO₂ snow clean [18].

4. Super-critical CO₂ has been proposed as an alternative cleaning method.
Because of its intrinsic physical properties such as absence of surface
sorption, high diffusion coefficient and high density, it has the characteristics
needed for good cleaning performance and penetration into narrow trenches
and vias. Stripping capabilities have been shown for post I/I applications
up to a dose of 2×10^{15} As/cm² [19–21]. The removal of crusted
resist is believed to be enhanced by the expansion upon pressure release:
a unique feature of this type of cleaning [19]. For BEOL post etch
residue removal it was shown that the use of scCO₂ cleaning leads to
superior electrical characteristics for BEOL 65 and 45nm technologies,
in comparison with the conventional O₂ based ashing and wet cleaning
approach [22].

5. Dissolution by liquid organic solvents has been proposed [23–25].
This approach is very attractive as solvents are expected not to attack
the materials such as Si, SiGe, SiO₂, metal gates and low-k dielectrics.
The solvents have to be selected to show optimal solubility for
photoresist. This choice is typically guided by different models that
represent molecular interactions and therefore determine solubility, such
as the Hansen solubility parameters [23, 26] or the Owens–Wendt
approach [27]. Obviously, in a final industrial implementation, ESH
criteria need to be fulfilled as well. Typically, the non-crosslinked bulk
of the photoresist can be removed, but not the crust itself [23, 26]
(Figure 8). Recently, this has been

![Figure 6. Carbon depth profiles (ToFSIMS) for blanket SiCN coated low k (30% porosity) reveal C-depletion at top surface. The various plasma treatments were applied to the low k prior to the dielectric SiCN barrier deposition.](image)

![Figure 7. Energy Filtered TEM reveals carbon depletion on sidewalls after etch and plasma treatment.](image)
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overcome by the use of megasonic agitation to the solvent (Figure 8) [26]. The latter approach was found to have promising properties also with regard to potential damage to fine up-features.

In summary, the approaches for PR removal can be classified in two categories. In a first approach the crust is chemically attacked and dissolved. Since this requires breaking of covalent bonds, very aggressive chemistry is required, typically involving radicals (similar to ashing). Particularly for low-k applications it is expected this may not yield sufficient selectivity.

In the second class, solid pieces of crust material are removed from the wafer. For such methods care needs to be taken to avoid redeposition and good removal of the crust material. This most likely requires frequent disposal of loaded chemical eventually in combination with appropriate filtration. This issue is comparable to a post-CMP cleaning and is therefore not expected to be a major roadblock. Therefore, it is highly desirable that knowledge on particle behaviour in solvents is developed [28].

**Conclusion**

Finally, it should be mentioned that photoresists are optimized firstly for lithographic patterning and secondly for endurance against dry etching (e.g. incorporation of P). The stripability receives less, if no attention, because these studies would require the use of various processes such as I/I and etching, which are often very process-specific and PR manufacturers may not have sufficient access to these processes. On the other hand PR manufacturers are very reluctant to disclose the nature of the photoresist materials. The search for optimized stripping would benefit significantly if these IP concerns could be accommodated. As an example, it could indeed ease the search for solvents of the non-crosslinked bulk and provide more insight into the nature of the crosslinking of the crust, and hence help to identify selective chemistries to break these links.

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**REFERENCES**

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Dr. Paul Mertens holds a Masters and a PhD degree of Applied Sciences from the KULeuven. He joined imec in 1984 to work on Silicon-on-insulator. From 1990 his main field of research is the investigation of the silicon wafer surface quality particularly for ULSI applications. This includes the quality of thin gate dielectrics, defect control, effects of contamination and cleaning processes and related metrology. Today Mertens is leading the Ultra Clean Processing program at imec. In this program, research on cleaning technology is conducted in collaboration with universities and ten leading edge IDMs.

He is an inventor of different processes and tools related to advanced wafer cleaning resulting in several patents and patent-applications. He presented at several scientific conferences, including several invited presentations, in the field of ultra clean processing, and authored and co-authored over 200 scientific papers in the field of silicon technology, mainly on issues related to advanced gate dielectrics, contamination effects and advanced wafer cleaning. He has been actively involved in the organization of the bi-annual international Ultra Clean Processing on Silicon Symposia (UCPSS) since its first edition in 1992, today recognized as a important forum for dissemination of knowledge on cleaning and contamination control.

Guy Vereecke received the M.S. degree in 1987 and the Ph.D. degree in 1999, both in Materials Sciences and from the Université Catholique de Louvain (UCL), Louvain-La-Neuve, Belgium. From 1987 to 1992 he was a researcher in the Laboratory for Chemistry of Interfaces of the UCL (Prof. P.G. Rouxhet), investigating the preparation of calcium phosphate biomaterials and the adsorption of proteins by various surface analysis techniques. In 1993 he joined the Ultra Clean Processing group of the Interuniversity Microelectronics Center (IMEC) where he is presently heading the BEOL cleaning team. He is author or co-author of more than 30 journal papers and 70 conference papers on surface analysis, gas phase contamination, dry cleaning, cleaning of nano-particles and damaging of structured wafers, CMP of advanced dielectrics, and wet strip and characterization of post-etch photoresist.

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