Introduction to Semiconductor Device Manufacturing

Semiconductor technology is continuously evolving and becoming more prevalent in our lives due to the significant advances in the technology and decreases in cost. One of the prominent trends in semiconductor technology over the last 40 years has been the shrinking in size of the individual transistors. This increases the number of transistors that can be included in each new generation of products.

The following narrative is a basic introduction to the semiconductor fabrication (commonly referred to as fab) manufacturing process.

Some of the most common electrical devices used in Integrated Circuits (IC) are transistors and capacitors. Both are manufactured by carving structures directly into the top of a wafer (slice of semiconductor material), as well as by depositing material on top of the wafer surface. A representative three dimensional top and side view of a transistor is shown below.

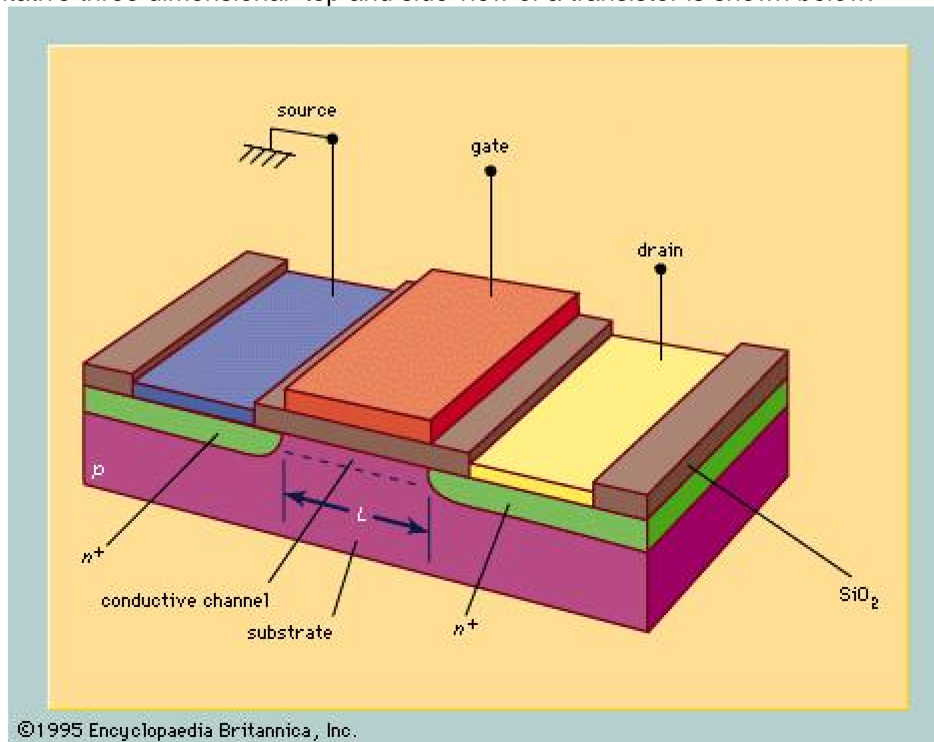

Figure 1: The Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET)
(http://electrons.wikidot.com/methods-for-the-determination-of-ground-state-wavefunction/comments/show)

The transistor operates as an electrical switch that is turned on or off by applying voltage to the gate electrode (the orange region). When a high enough voltage is applied to the gate, an electrical current flows between the source (green region below the blue region) and the drain (green region below the yellow region).

In semiconductor manufacturing, ICs are often made from large silicon wafers. Following the processing in the fabrication line, wafers are broken down into many identical dies. Each die can contain millions of transistors and is packaged separately.

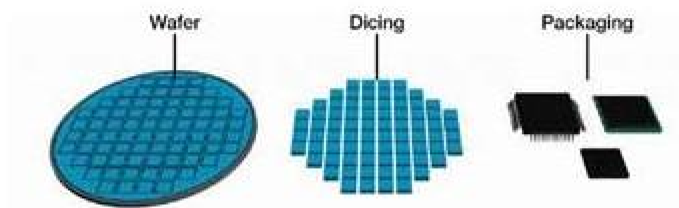

Figure 2: From processed wafer to packaged dies

The transistor shown in figure 1 is a fully manufactured transistor that is typically fabricated in the following sequence:

1. An oxide layer such as SiO_2 (brown regions) is grown across the top surface of the planar silicon substrate wafer (purple region).
2. A conductive layer such as polysilicon or a metal is then deposited across the entire oxide layer. Most of this material, shown in orange in Figure 1, will soon be etched away, leaving just the gate.
3. Following the depositions on the surface, a pattern will be formed using photolithography. Photolithography includes the following set of processes that creates physical structures on top of the wafer:
    a. Spin a photoresist onto the wafer.
    b. The photoresist is exposed to a light source through a patterned mask (e.g. by using a sophisticated light projector such as stepper).
    c. The unexposed photoresist is then chemically removed.
4. The polysilicon (or metal) and the oxide are etched from the areas where the photoresist was removed; these locations will become the source and drain (green)
5. In order to create the doped green regions in the purple p+ substrate, ions are implanted through an opening in the oxide.
6. The ion implanted dopants get activated in a heat treatment in an oven, making the source and drain functional.
7. A second mask is used to create the gate electrode by patterning just the top polysilicon or a metal layer (in a process similar to step # 3), leaving the other layers untouched.
8. In order to isolate and protect the finalized electrical components, an isolation dielectric is deposited on top of the surface shown in figure 1.
9. Holes are drilled in the dielectric material, followed by deposition of metal plugs and metal conductor lines to connect the electrodes within an IC.

10. A final protective dielectric layer (passivation) is deposited on the metal lines to keep the electrical component isolated.

The sequence described above is a basic procedure that is used many times repetitively in semiconductor processing. For example, steps 1 through 7 can be repeated many times on a single chip to create varieties of transistors, depending on the conditions used during manufacturing. Changing the type of dopants implanted in step 5 creates a different type of transistor since the dopants affect the electrical properties of the component. As steps 1 through 7 are repeated, more metal layers are needed to connect them; this can be done by repeating steps 8 through 10.

In modern semiconductor fabrication, the actual fab process is much more complex than this basic illustration. For example, a cross section of a 512Mb DRAM memory device made with two metal and two polysilicon layers is shown below. As this image indicates, applications for various chips require significant additions to the processing steps 1 through 10. Regardless, any fabrication of basic electrical components is based on the fundamental process described above.

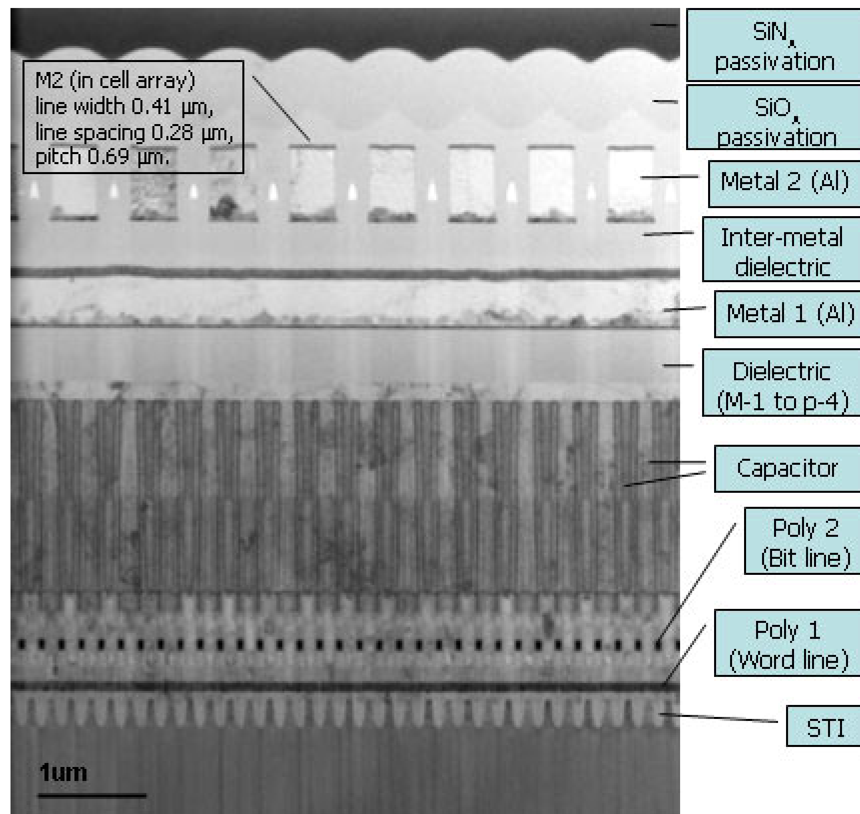

Figure 3: Samsung 512Mb DRAM Cross section
(http://www.ma-tek.com/industry_detail.php?cpath=23)

Additional Resources:

1. News and Technical Article about Semiconductor Manufacturing

2. New Process Technology
3. International Technology Roadmap for Semiconductors (ITRS)
4. In-Depth Articles on the Semiconductor Manufacturing Process
5. Semiconductor Technical Glossary
6. Semiconductor Industry Resources